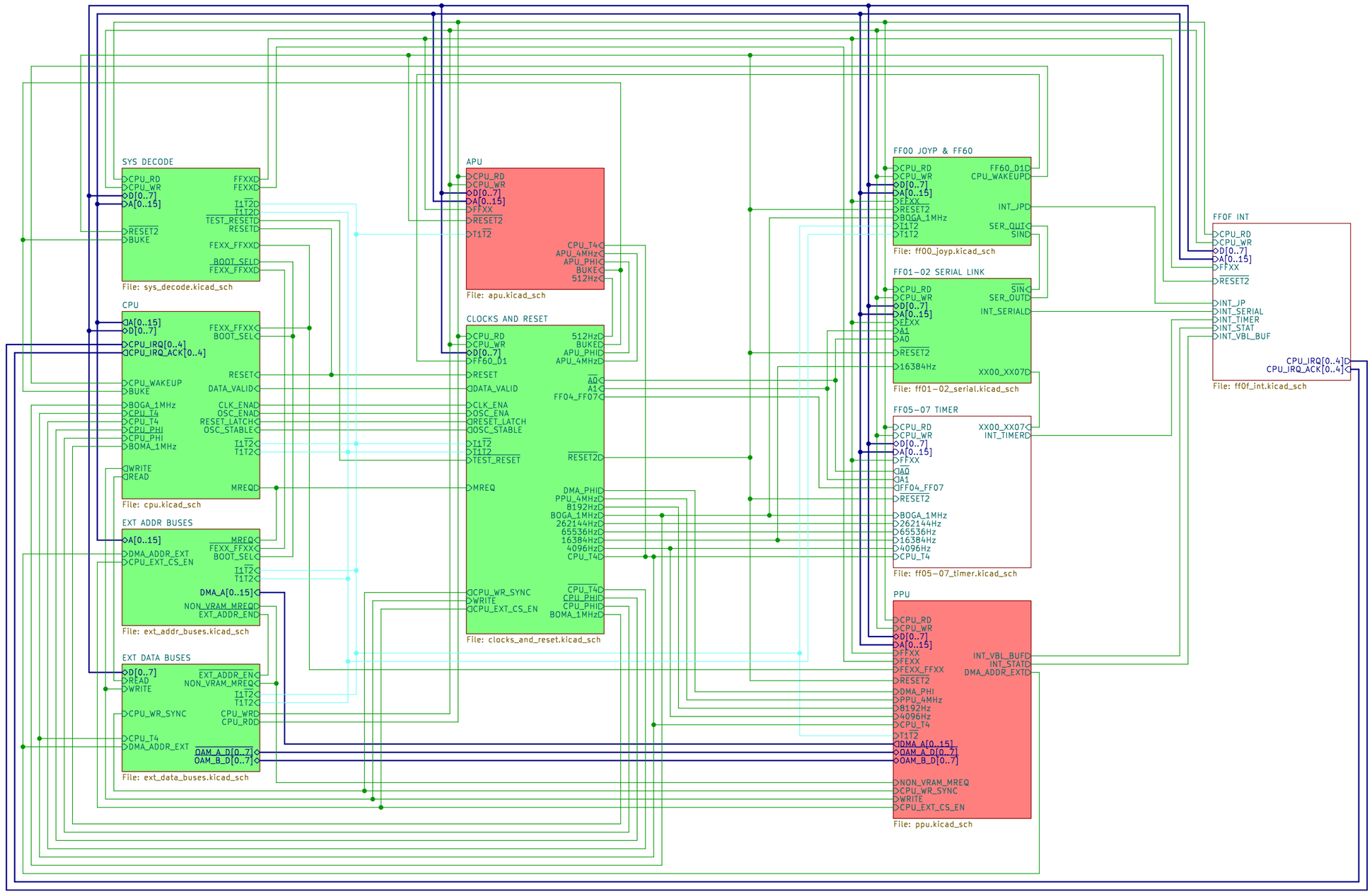


Green boxes contain IO pins
Red boxes contain sub sheets

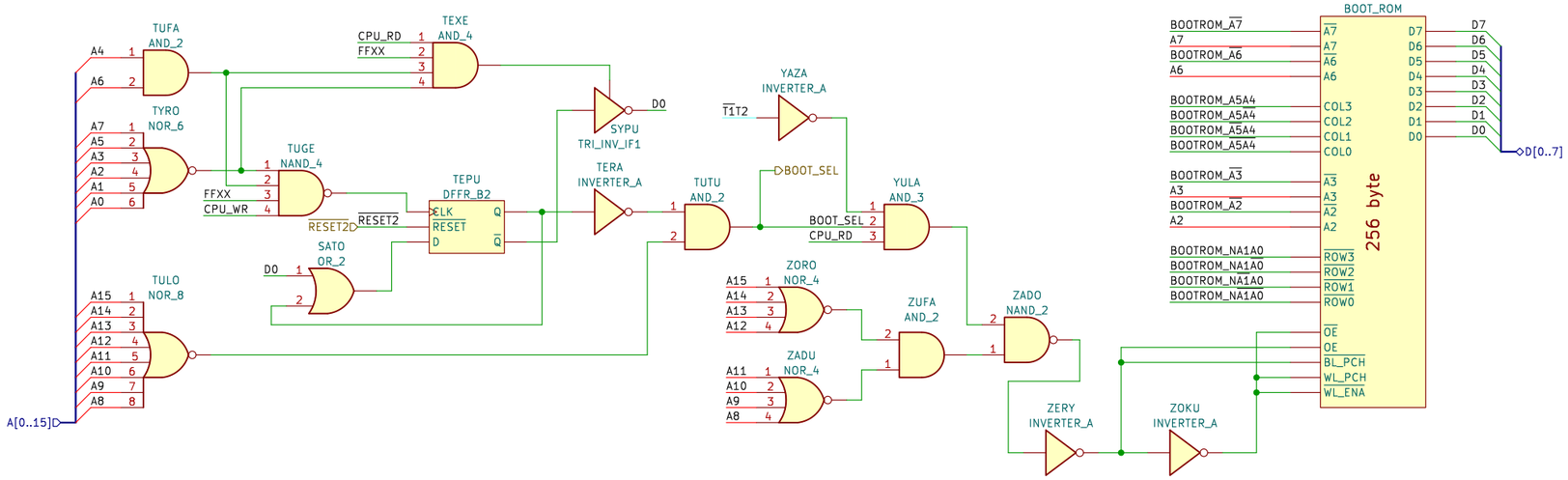
https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

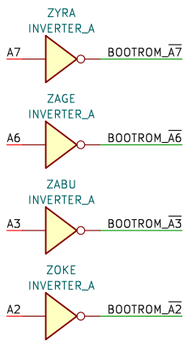
Sheet: /
File: dmg_cpu_b.kicad_sch

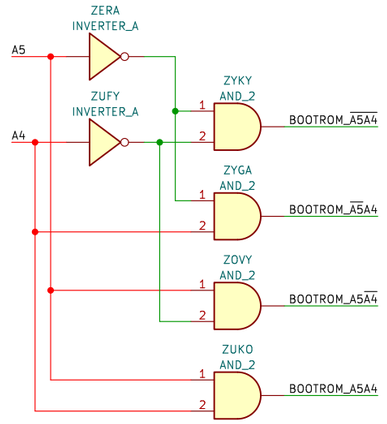
Title: DMG-CPU B

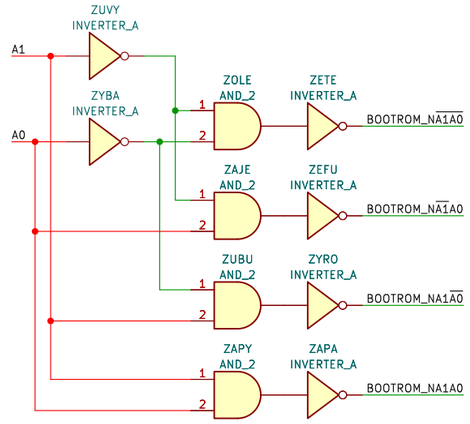
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 1/46

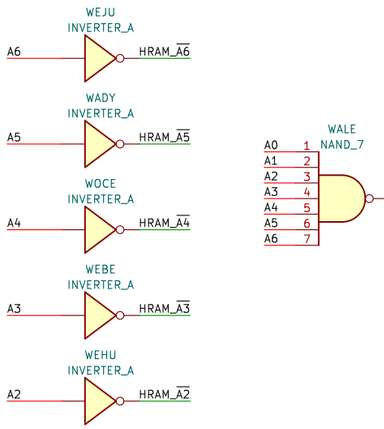
FF50 BOOT EN

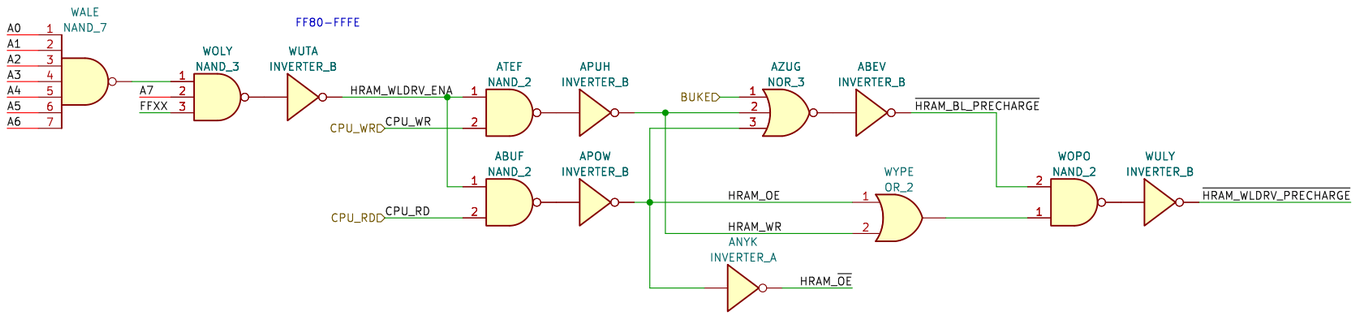


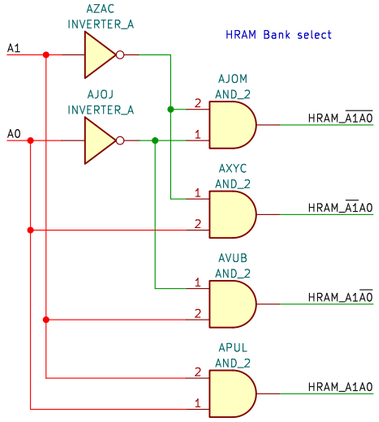


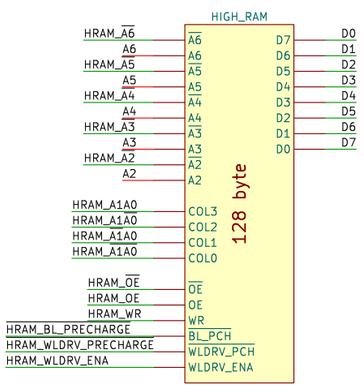


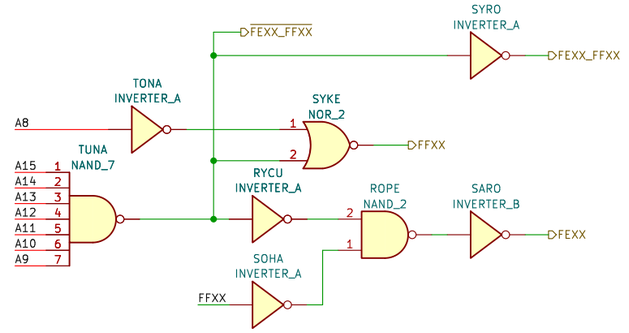


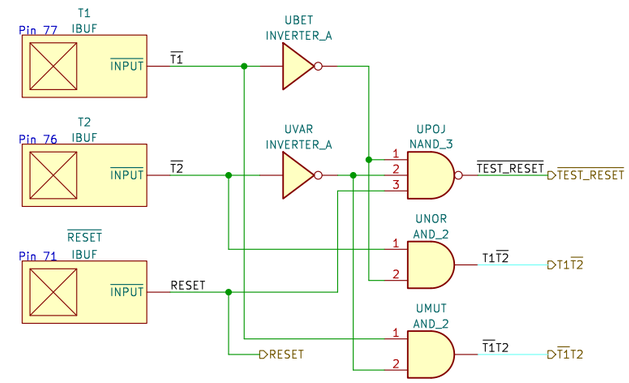










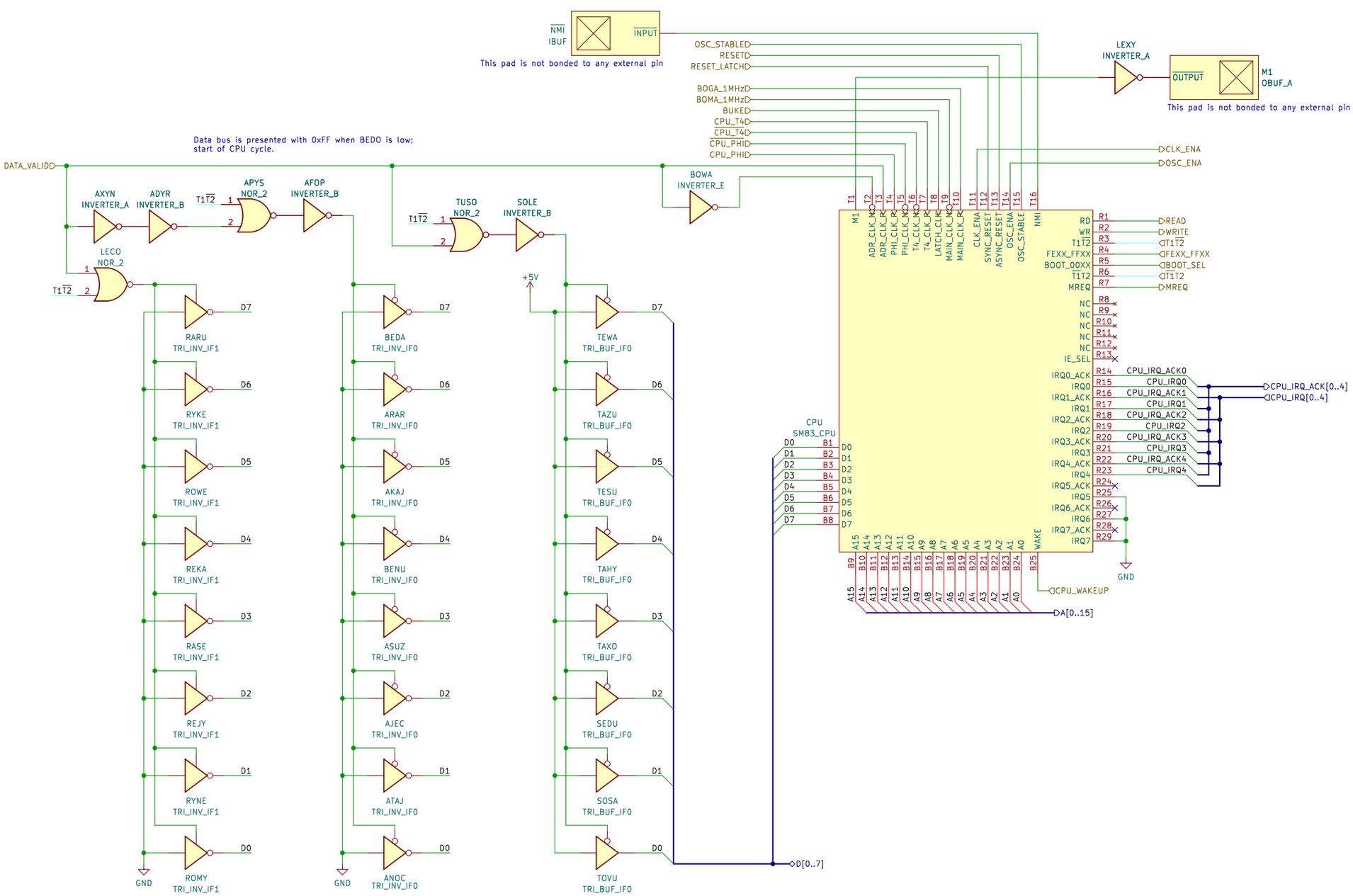


In normal mode, T1 and T2 pins are gounded on PCB, so T1T2 and T1T2 are always low.
TEST_RESET only goes low when T1=T2=1 and RESET=0.
T1 and/or T2 are set to 1 for test modes.

Sheet: /SYS DECODE/
File: sys_decode.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 2/46



Sheet: /CPU/
File: cpu.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 3/46

TYNU = '1' when A >= 0xA000 else '0'.
TOZA = '1' when A >= 0xA000 and < 0xFE00; RAM space
RAM_CS can only go low in RAM space when driven by CPU

TEXO = '1' during mem req access when A < 0x8000 or A >= 0xA000 else '0'.
It excludes the VRAM address range.
A0–14 are latched and presented to external pins when driven by CPU

SOGY INVERTER_A
TUMA AND_3
TYNU AO_1
SOBY NOR_2
TOZA AND_3
SEPY NAND_2
RYCA INVERTER_A
TOVA INVERTER_A
TYHO MUX
TAZY MUX
PEGE MUX
MUCE MUX
MOJY MUX
MALE MUX
PAMY MUX
MASU MUX
MANO MUX
MULE INVERTER_A
LOXO AO_1
LASY INVERTER_A
MATE INVERTER_A
SORE INVERTER_A
TEVY OR_3
TEXO AND_2
NYRE D_LATCH_B
LONU D_LATCH_B
LOBU D_LATCH_B
LUMY D_LATCH_B
PATE D_LATCH_B
LYSA D_LATCH_B
LUNO D_LATCH_B
RULO NOR_2
SUZE NAND_2
RAZA INVERTER_A
SYZU TRI_BUF_IF0
PAHY NOR_2
PUHE NAND_2
PEVO INVERTER_A
NEFE TRI_BUF_IF0
LEVA NOR_2
LABE NAND_2
LURA INVERTER_A
LEFY TRI_BUF_IF0
LOSO NOR_2
LUCE NAND_2
LAHE INVERTER_A
LYNA TRI_BUF_IF0
LYNY NOR_2
LEPY NAND_2
MADY INVERTER_A
LORA TRI_BUF_IF0
RORE NOR_2
ROXU NAND_2
SURA INVERTER_A
RALA TRI_BUF_IF0
MENY NOR_2
MUNE NAND_2
NENA INVERTER_A
MAPU TRI_BUF_IF0
MEGO NOR_2
MYNY NAND_2
MUJY INVERTER_A
LOFA TRI_BUF_IF0
ARYM D_LATCH_B
AROS D_LATCH_B
ATEV D_LATCH_B
AVYS D_LATCH_B
ARET D_LATCH_B
ALYR D_LATCH_B
APUR D_LATCH_B
ALOR D_LATCH_B
ASUR MUX
ATYR MUX
ATOV MUX
ATEM MUX
AMER MUX
APOK MUX
ATOL MUX
AMET MUX
COLO NOR_2
DEFY NAND_2
COGO INVERTER_A
CYKA NOR_2
CEPU NAND_2
CYGU INVERTER_A
AJAV NOR_2
BADU NAND_2
ABUP INVERTER_A
BEVO NOR_2
BYLA NAND_2
AFEC INVERTER_A
BOLA NOR_2
BOTY NAND_2
BASE INVERTER_A
BAJO NOR_2
BOKU NAND_2
BUXU INVERTER_A
COTU NOR_2
CABA NAND_2
CAMU INVERTER_A
KOTY NOR_2
KUPO NAND_2
KOVA INVERTER_A
BYNA TRI_BUF_IF0
BYNE TRI_BUF_IF0
AJOV TRI_BUF_IF0
AZUV TRI_BUF_IF0
ANAR TRI_BUF_IF0
AKAN TRI_BUF_IF0
BYXE TRI_BUF_IF0
KEJO TRI_BUF_IF0

DMA_ADDR_EXT
DMA_A15
DMA_A14
DMA_A13
DMA_A12
DMA_A11
DMA_A10
DMA_A9
DMA_A8
DMA_A7
DMA_A6
DMA_A5
DMA_A4
DMA_A3
DMA_A2
DMA_A1
DMA_A0
DMA_ADDR_EXT
EXT_ADDR_EN
EXT_A15_EN
ADDR_LATCH
T1T2
MREQ
AXXX–FXXX
CPU_EXT_CS_END
FEXX_FFXX
BOOT_SELL
NON_VRAM_MREQ
DMA_A[0..15]
A[0..15]
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
OUTPUT
DRV_LOW
DRV_HIGH
INPUT
ENA
D
Q
A15 IOBUF_A Pin 16
A14 IOBUF_A Pin 15
A13 IOBUF_A Pin 14
A12 IOBUF_A Pin 13
A11 IOBUF_A Pin 12
A10 IOBUF_A Pin 11
A9 IOBUF_A Pin 10
A8 IOBUF_A Pin 9
A7 IOBUF_A Pin 8
A6 IOBUF_A Pin 7
A5 IOBUF_A Pin 6
A4 IOBUF_A Pin 5
A3 IOBUF_A Pin 4
A2 IOBUF_A Pin 3
A1 IOBUF_A Pin 2
A0 IOBUF_A Pin 1

Sheet: /EXT ADDR BUSES/
File: ext_addr_buses.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 4/46

T1T2 test mode makes RD and WR inputs to bypass the CPU

D[0..7]

OAM_A_D[0..7]

OAM_B_D[0..7]

Sheet: /EXT DATA BUSES/
File: ext_data_buses.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 5/46

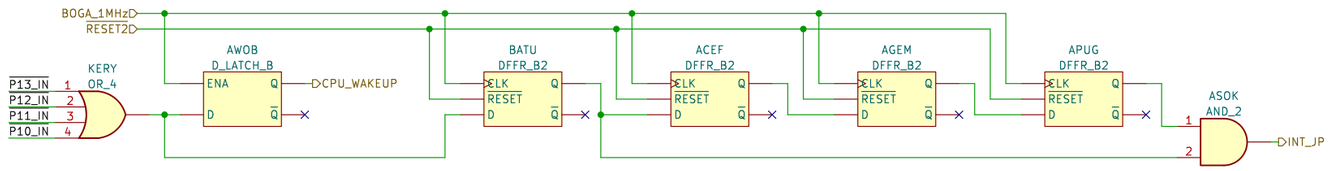
FF04 DIV

CLK_ENA
BAPY NOR_3
BERU INVERTER_B
BELU NOR_2
BYRY INVERTER_B
BUFA INVERTER_D
BYLY INVERTER_E
BOLO INVERTER_D
BYDA INVERTER_E
BUDE INVERTER_D
BEVA INVERTER_E
BEKO INVERTER_D
BAVY INVERTER_E
CPU_T4
CPU_T4
BEJA NAND_4
BANE INVERTER_A
BELO INVERTER_A
BAZE INVERTER_A
BUTO NAND_3
CPU_PHI
CPU_PHI
OUTPUT
PHI OBUF_A
Pin 75
DOVA INVERTER_D
APU_PHI
UVYT INVERTER_B
DMA_PHI
BELE INVERTER_A
ATEZ INVERTER_A
BYJU OR_2
BALY INVERTER_A
BOGA INVERTER_E
BOMA INVERTER_E
BOMA_1MHz
BOGA_1MHz
BOGA_1MHz
TEST_RESET
AFER DFFR_B
RESET_LATCH
AVOR OR_2
ALUR INVERTER_B
RESET2
ABOL INVERTER_A
CLK_ENA
BUTY INVERTER_A
BUVU AND_2
BYXO INVERTER_A
BEDO INVERTER_E
DATA_VALID
CLK_ENA
UPOF DFFR_B2
UKET DFFR_B2
TEKA DFFR_B2
SUBU DFFR_B2
SOLA DFFR_B2
TERU DFFR_B2
TOFE DFFR_B2
TUGO DFFR_B2
TULU DFFR_B2
UGOT DFFR_B2
RESET
UPYF OR_2
TUBO NOR_LATCH
T1T2
T1T2
UNUT AND_2
TABA OR_3
OSC_STABLE
ALYP INVERTER_A
AFAR NOR_2
ASOL NOR_LATCH
RESETD
RESET
16Hz
FF04_FF07
CPU_RD
A1
A0
TAGY AND_4
Read to FF04 return counter value
OSC_ENA
OSC_ENA
UCOB INVERTER_A
FF04_FF07
CPU_WR
A1
A0
TAPE AND_4
Write to FF04 resets counter
RESET
UFOL NOR_3
RESET_DIV
UDOR INVERTER_A
RYSO INVERTER_A
RAVE INVERTER_A
UMER INVERTER_A
SAPY INVERTER_A
UTOK INVERTER_A
UREK INVERTER_A
UMEK INVERTER_A
512Hz
512Hz
4096Hz
8192Hz
TATU TRI_INV_IF1
SAWA TRI_INV_IF1
SEPU TRI_INV_IF1
UPUG TRI_INV_IF1
TUSE TRI_INV_IF1
TEMU TRI_INV_IF1
TAKU TRI_INV_IF1
TAWU TRI_INV_IF1
D7
D6
D5
D4
D3
D2
D1
D0
D[0..7]
ADEH INVERTER_A
ADYK DR_LATCH
ADAR INVERTER_A
AFAS NOR_2
AREV NAND_2
APOV INVERTER_C
CPU_WR_SYNC
WRITED
AFUR DR_LATCH
ATYP INVERTER_A
AJAX INVERTER_A
AGUT OA
AWOD NOR_2
ABUZ INVERTER_C
CPU_EXT_CS_EN
MREQD
T1T2
T1T2
ALEF DR_LATCH
AFEP INVERTER_A
BUGO INVERTER_A
BATE NOR_3
BASU INVERTER_A
BUKE INVERTER_E
BUKE
CLK_ENA
APUK DR_LATCH
AROV INVERTER_A
TEST_RESET
TEST_RESET
ATAL_4MHz
ATAG INVERTER_A
AMUK INVERTER_E
APU_4MHz
ANOS NAND_2
CK1_CK2 OSC
ARYS INVERTER_A
AVET NAND_2
ATAL INVERTER_B
AZOF INVERTER_E
ZAXY INVERTER_B
ZEME INVERTER_D
PPU_4MHz
CLK
ENA
OSC_ENA
Pin 74 (CK1) is input
Pin 73 (CK2) is output
TAMA DFFR_B2
UNYK DFFR_B2
TERO DFFR_B2
UNER DFFR_B2
UFOR DFFR_B2
UKUP DFFR_B2
UVYN INVERTER_A
UVYR INVERTER_A
UBOT INVERTER_A
16384Hz
65536Hz
262144Hz
BOGA_1MHz
FF60_D1
BOGA_1MHz
ULUR MUX

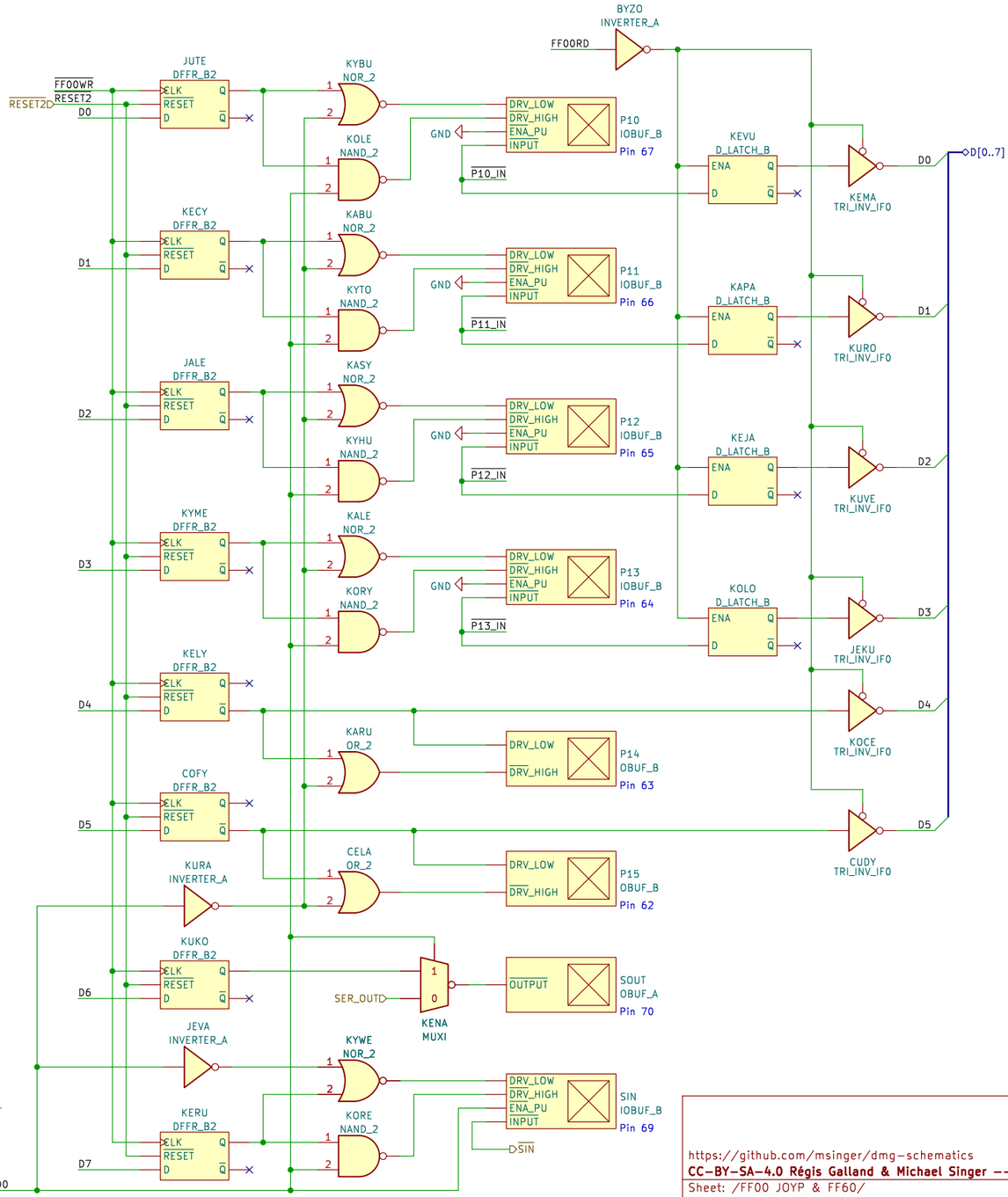
Sheet: /CLOCKS AND RESET/
File: clocks_and_reset.kicad_sch

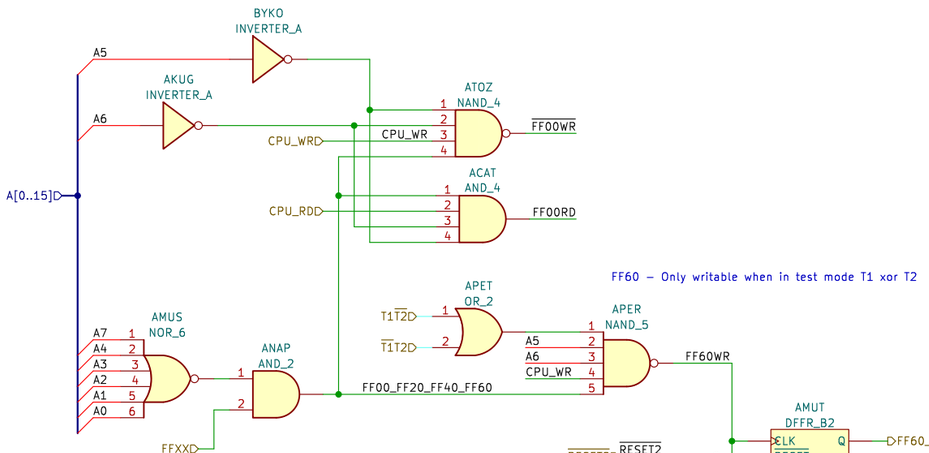
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 6/46

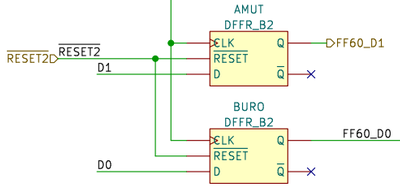


FF00 JP





FF60 — Only writable when in test mode T1 xor T2



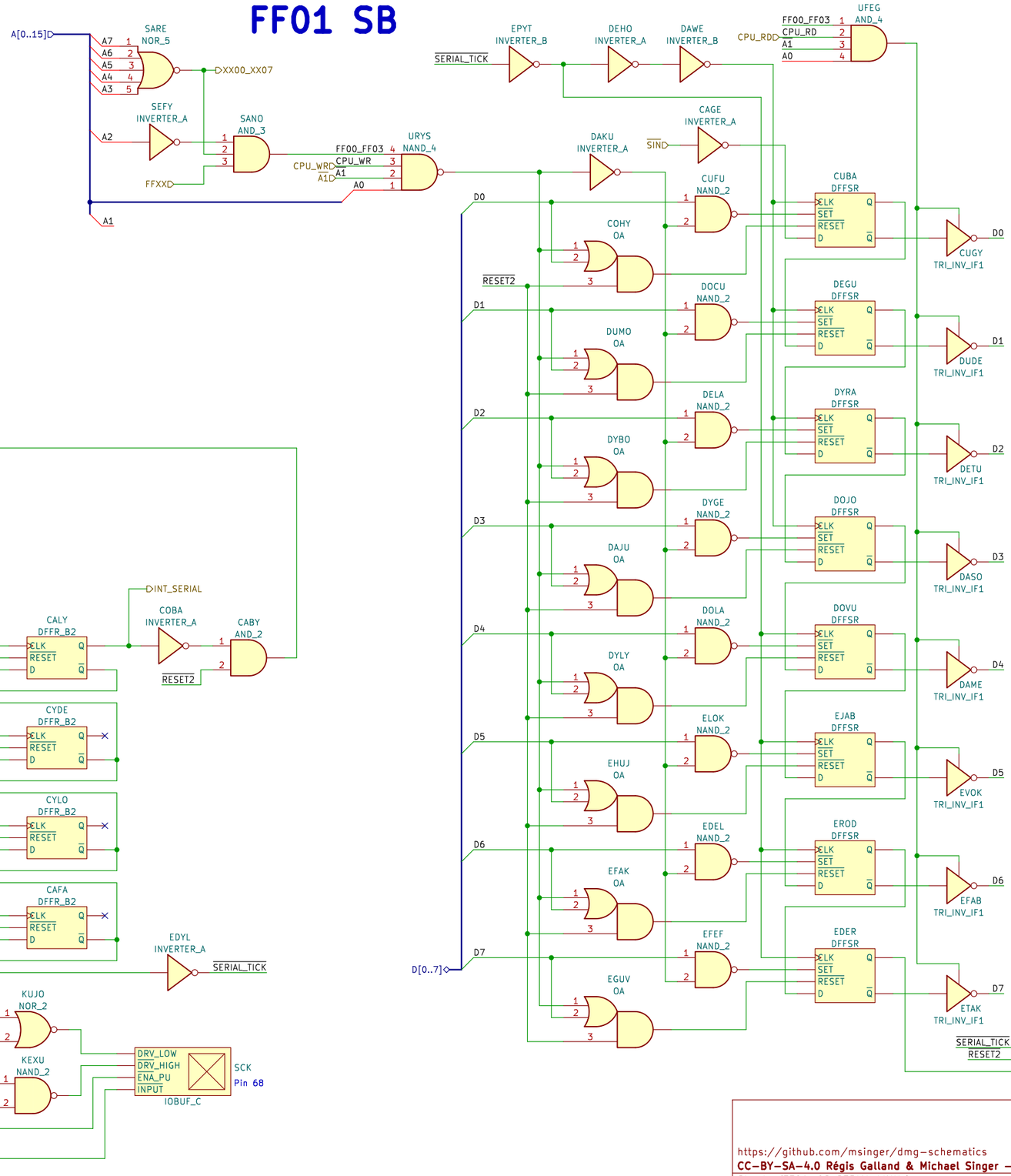
FF60

Sheet: /FF00 JOYP & FF60/
File: ff00_joyp.kicad_sch

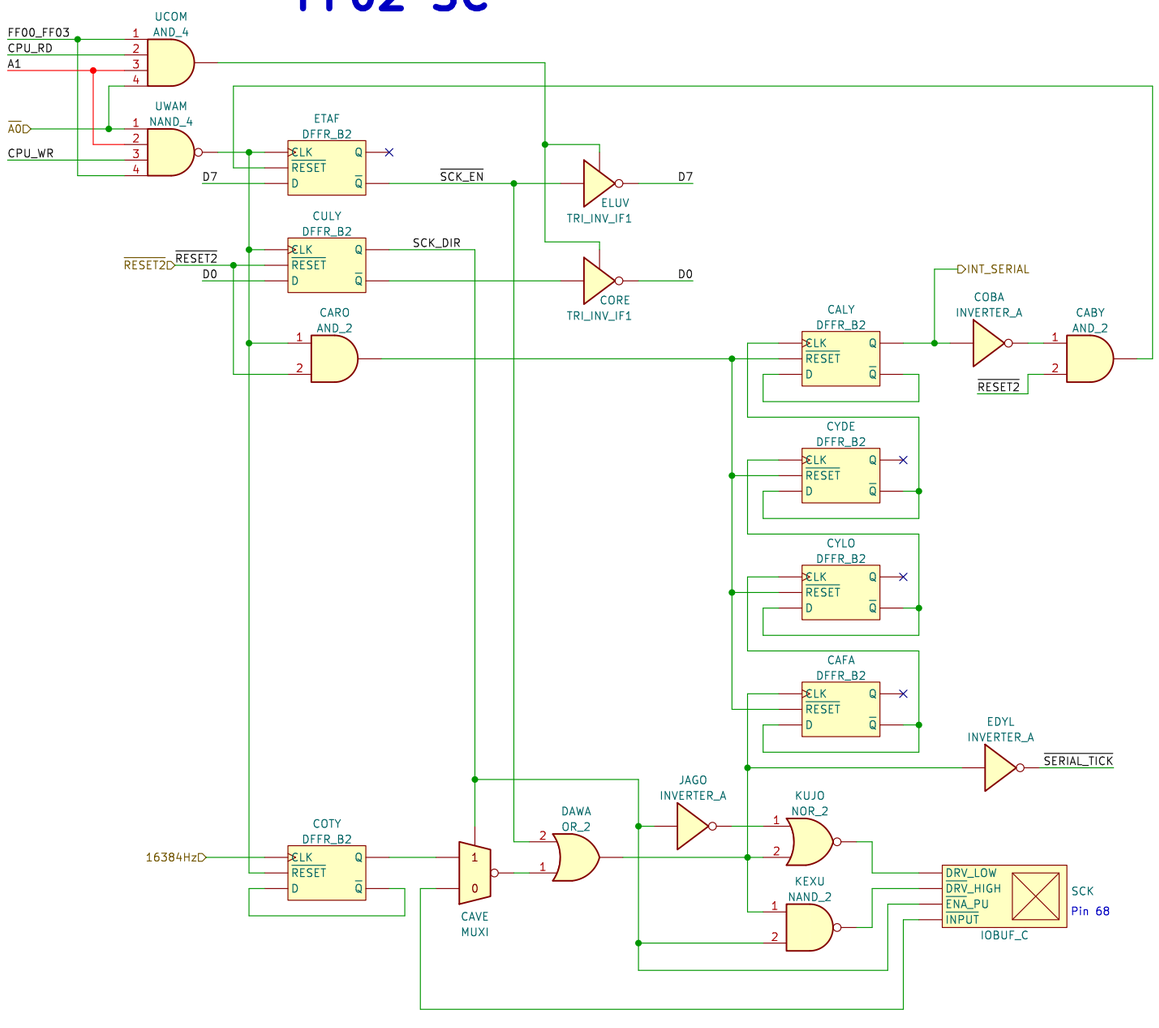
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 7/46

FF01 SB

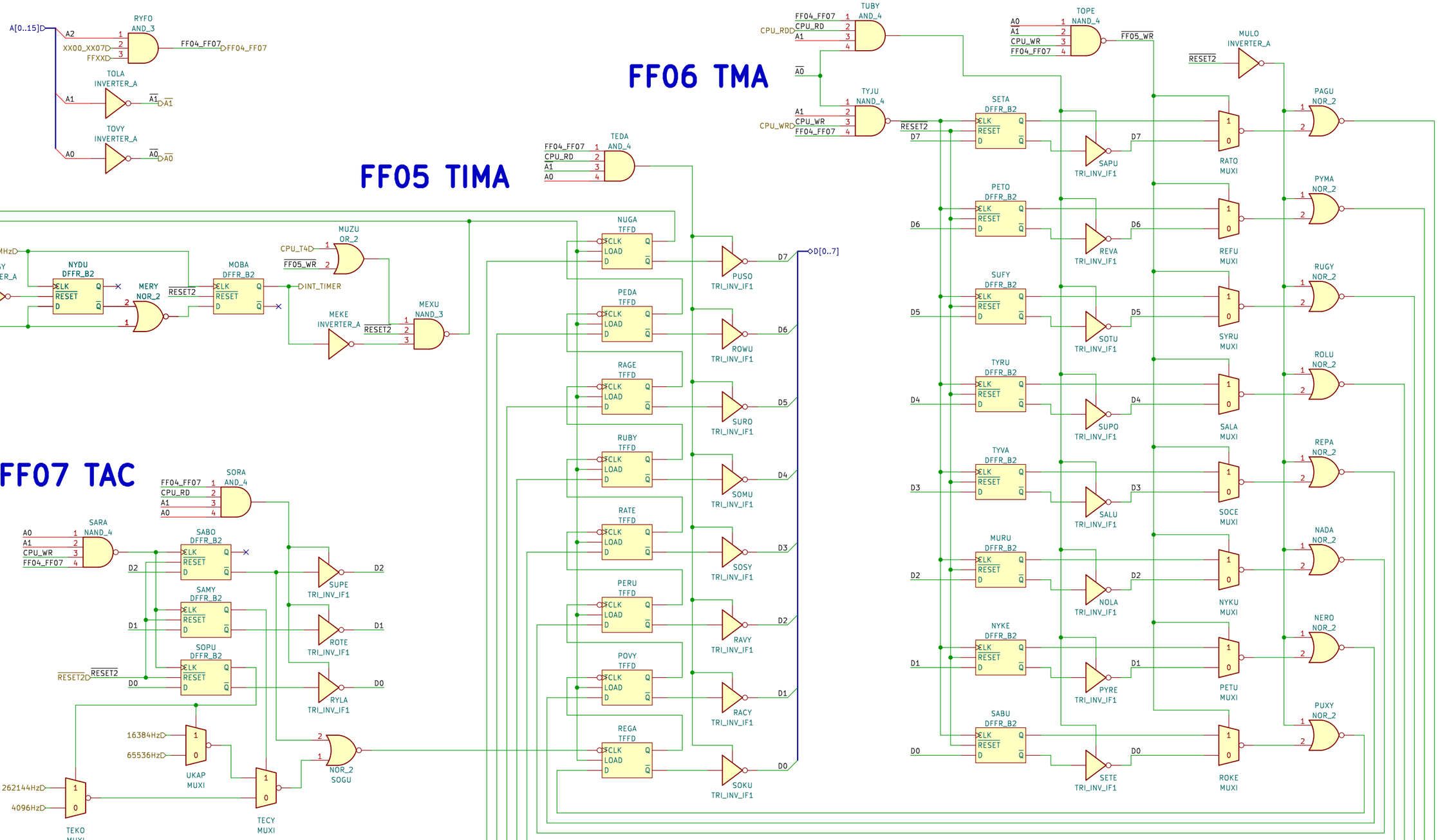


FF02 SC



Sheet: /FF01-02 SERIAL LINK/		
File: ff01-02_serial.kicad_sch		
Title: DMG-CPU B		
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 8/46

FF06 TMA



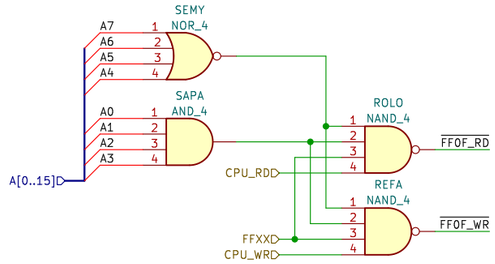
FF05 TIMA

FF07 TAC

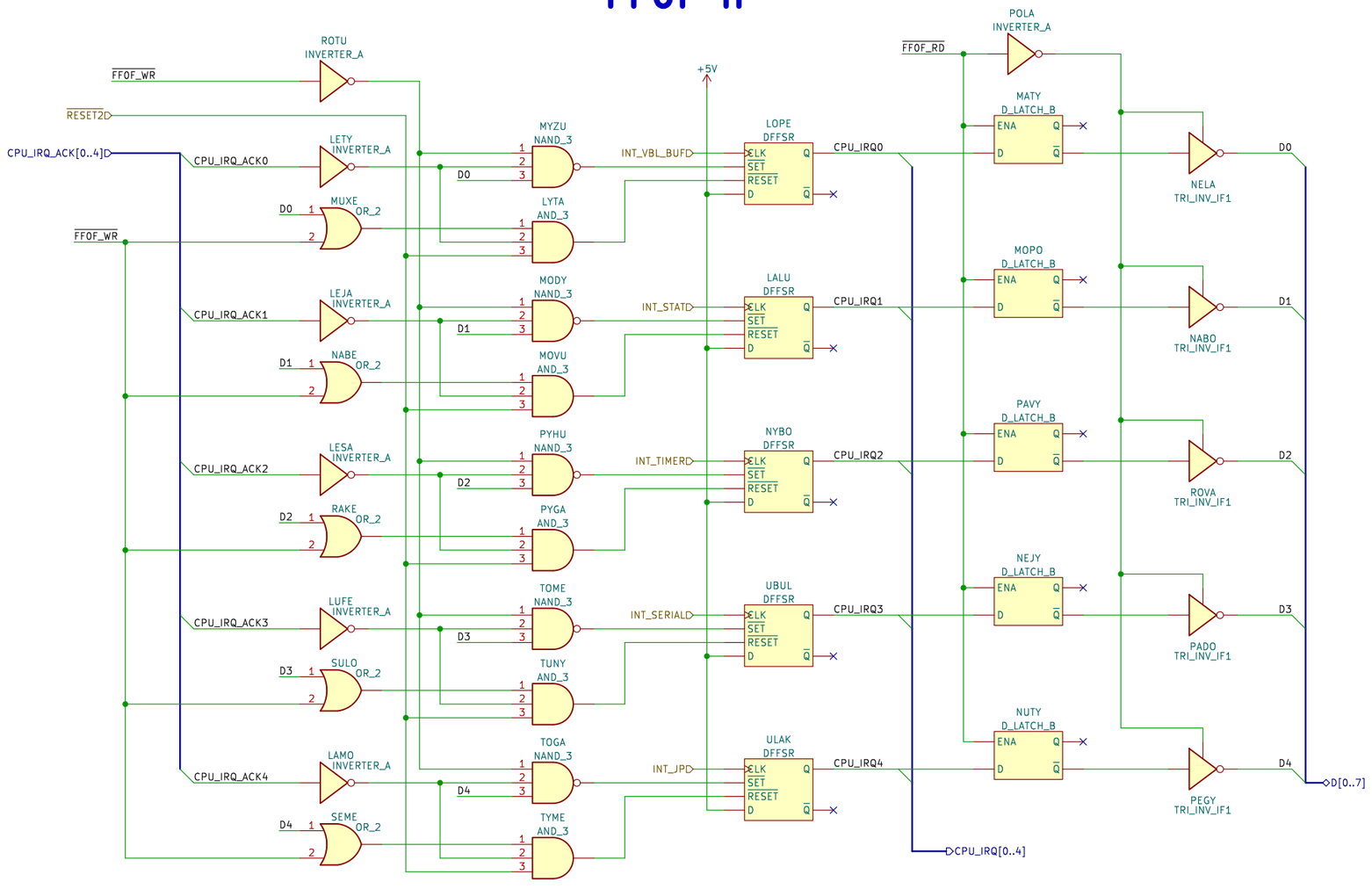
Sheet: /FF05-07 TIMER/
File: ff05-07_timer.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 9/46



FFOF IF



Sheet: /FFOF INT/		
File: ff0f_int.kicad_sch		
Title: DMG-CPU B		
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 10/46

APU DECODE

File: apu_decode.kicad_sch

File: ff24_ff25.kicad_sch

File: apu_control.kicad_sch

File: ch1_regs.kicad_sch

File: ch1_sweep.kicad_sch

File: channel1.kicad_sch

File: ch2_regs.kicad_sch

File: channel2.kicad_sch

File: ch3_regs.kicad_sch

File: ch3_wave_ram.kicad_sch

File: ch4_regs.kicad_sch

File: channel4.kicad_sch

https://github.com/msinger/dmg-schematics

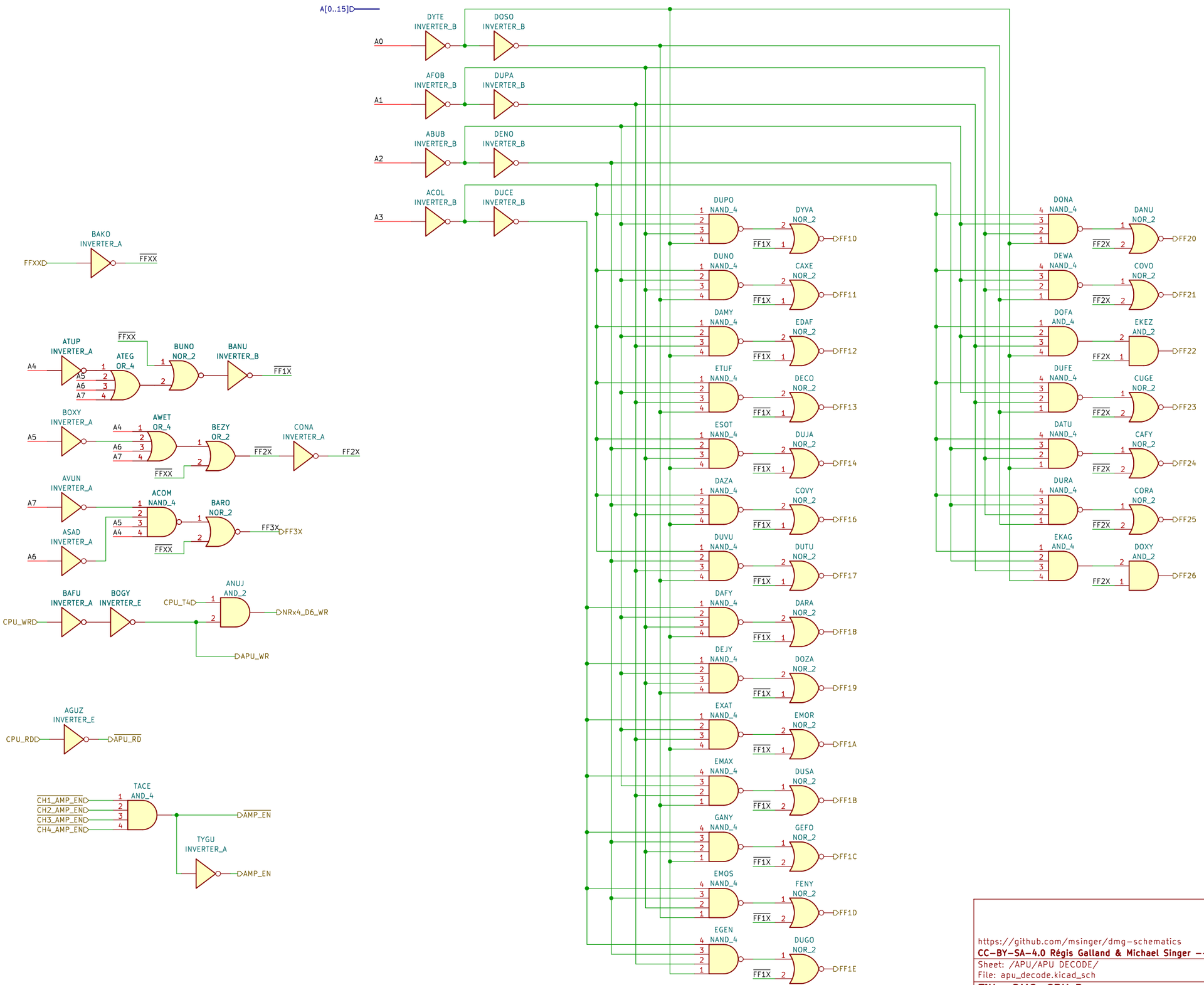
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

Sheet: /APU/

File: apu.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 11/46



https://github.com/msinger/dmg-schematics

CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

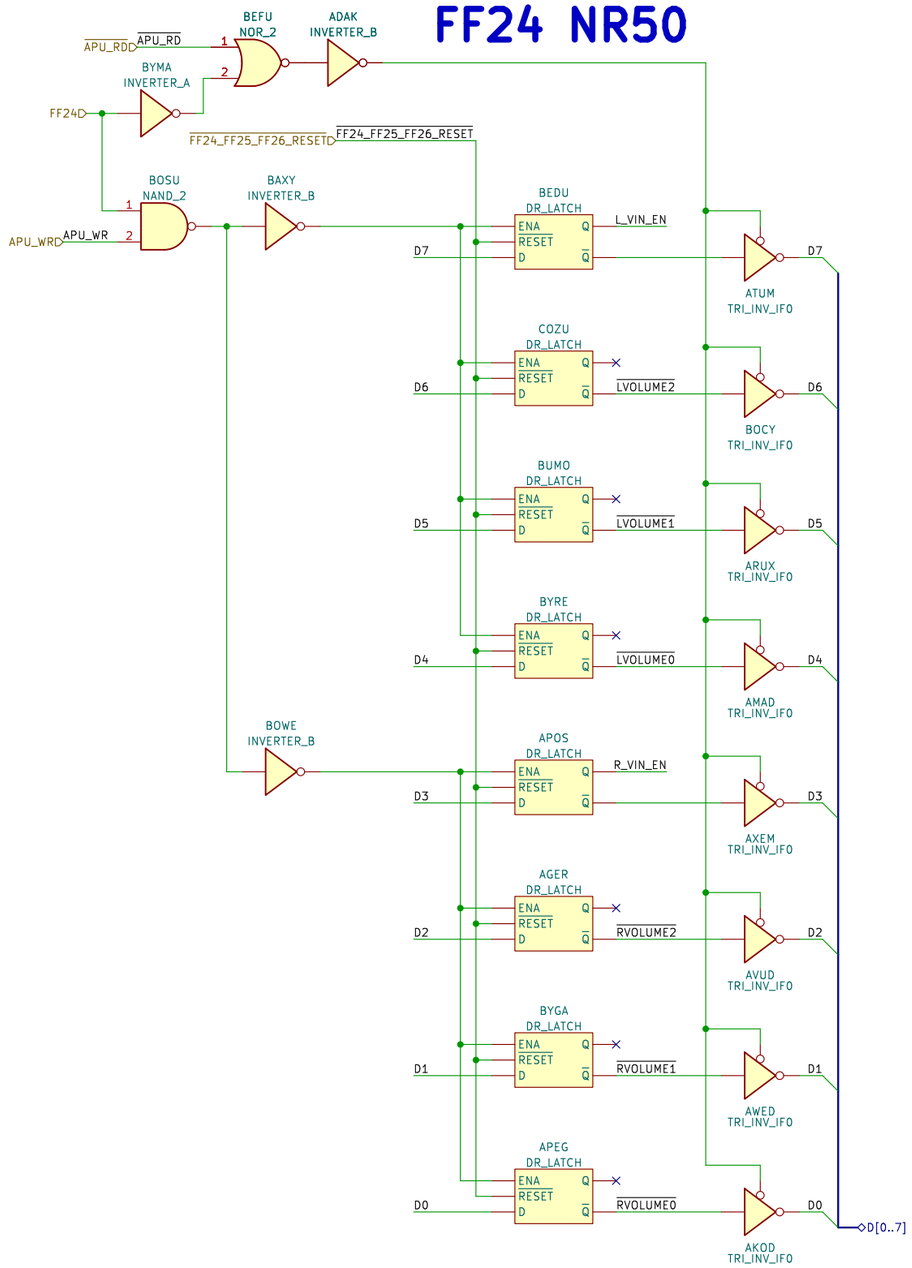
Sheet: /APU/APU DECODE/

File: apu_decode.kicad_sch

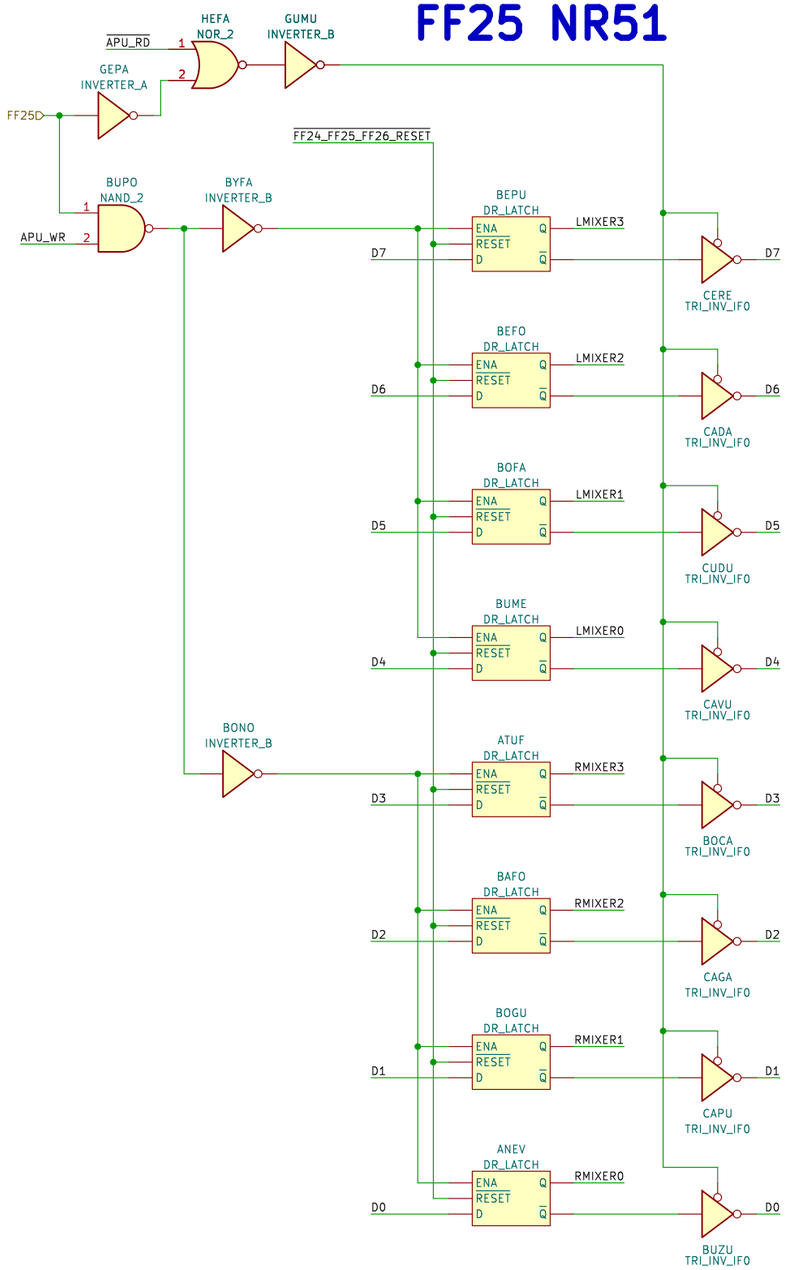
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 12/46

FF24 NR50



FF25 NR51

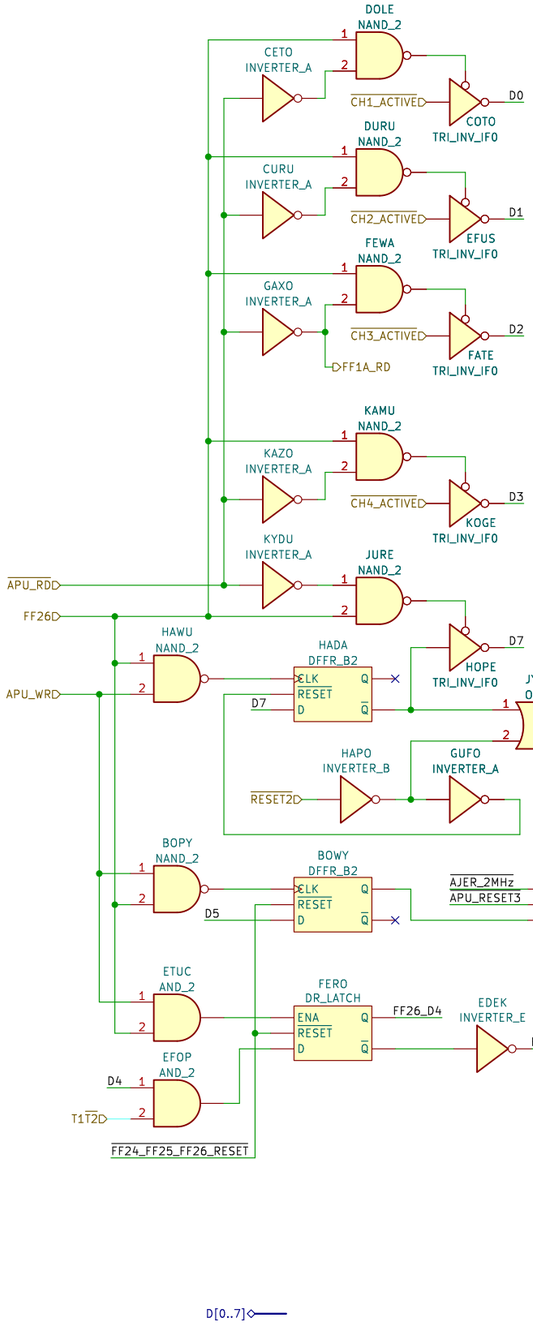


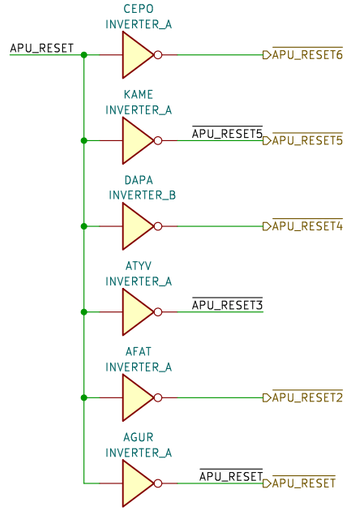
Sheet: /APU/FF24 FF25 CH EN & VOL/
File: ff24_ff25.kicad_sch

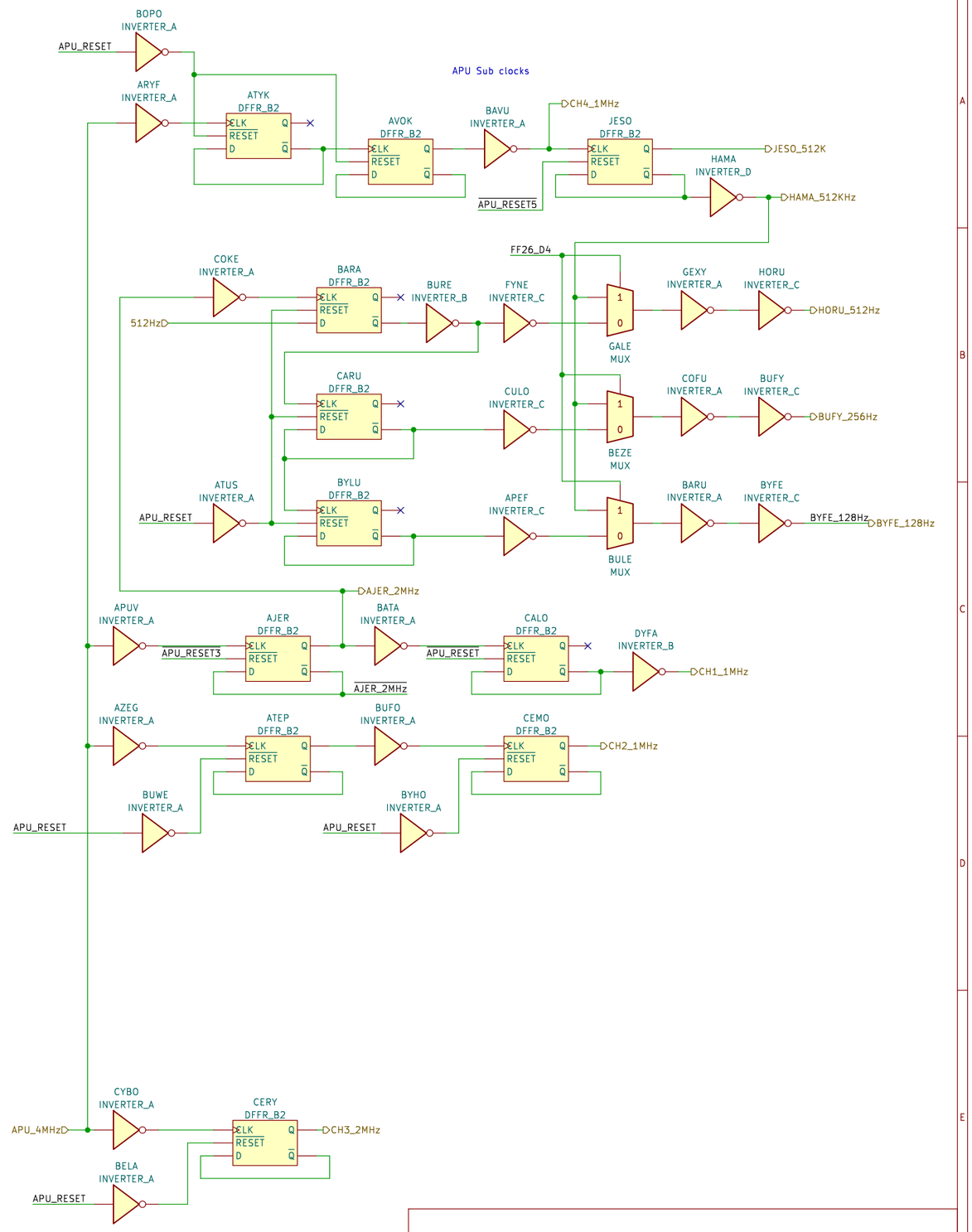
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 13/46

FF26 NR52





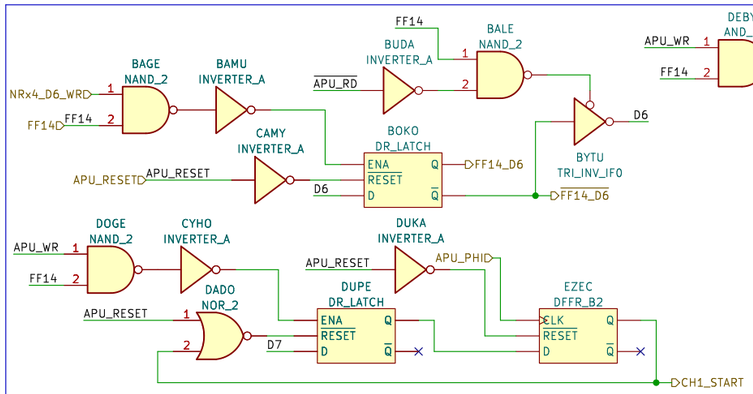


Sheet: /APU/FF26 APU CLOCKS & RESETS/
File: apu_control.kicad_sch

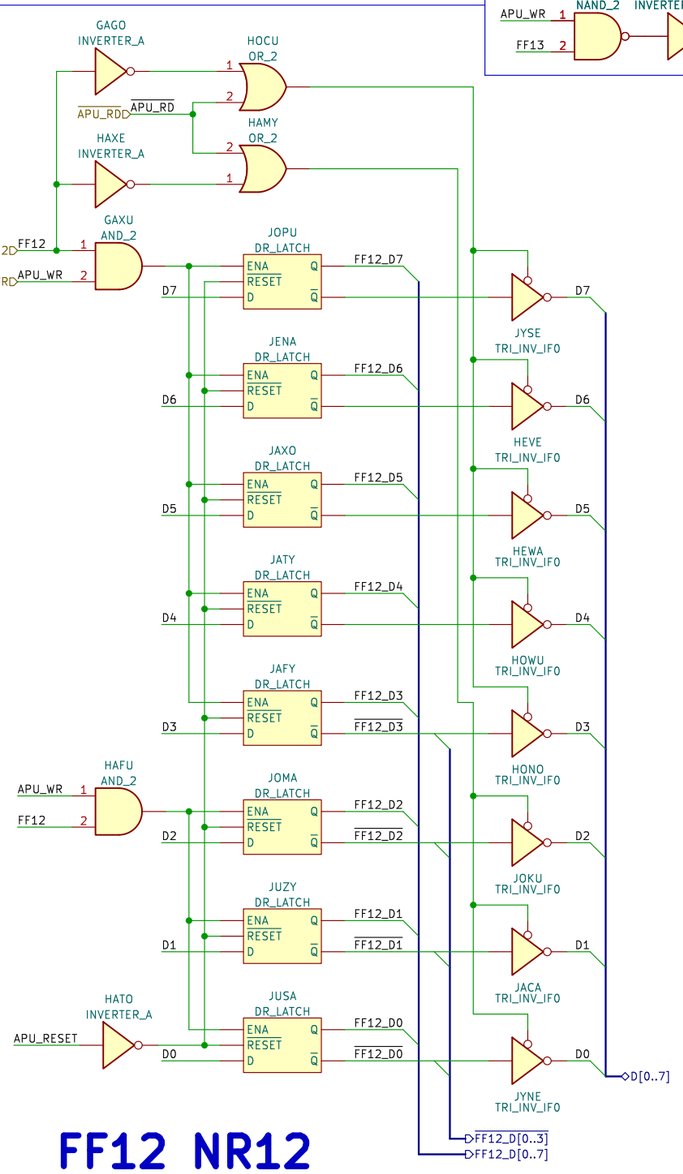
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 14/46

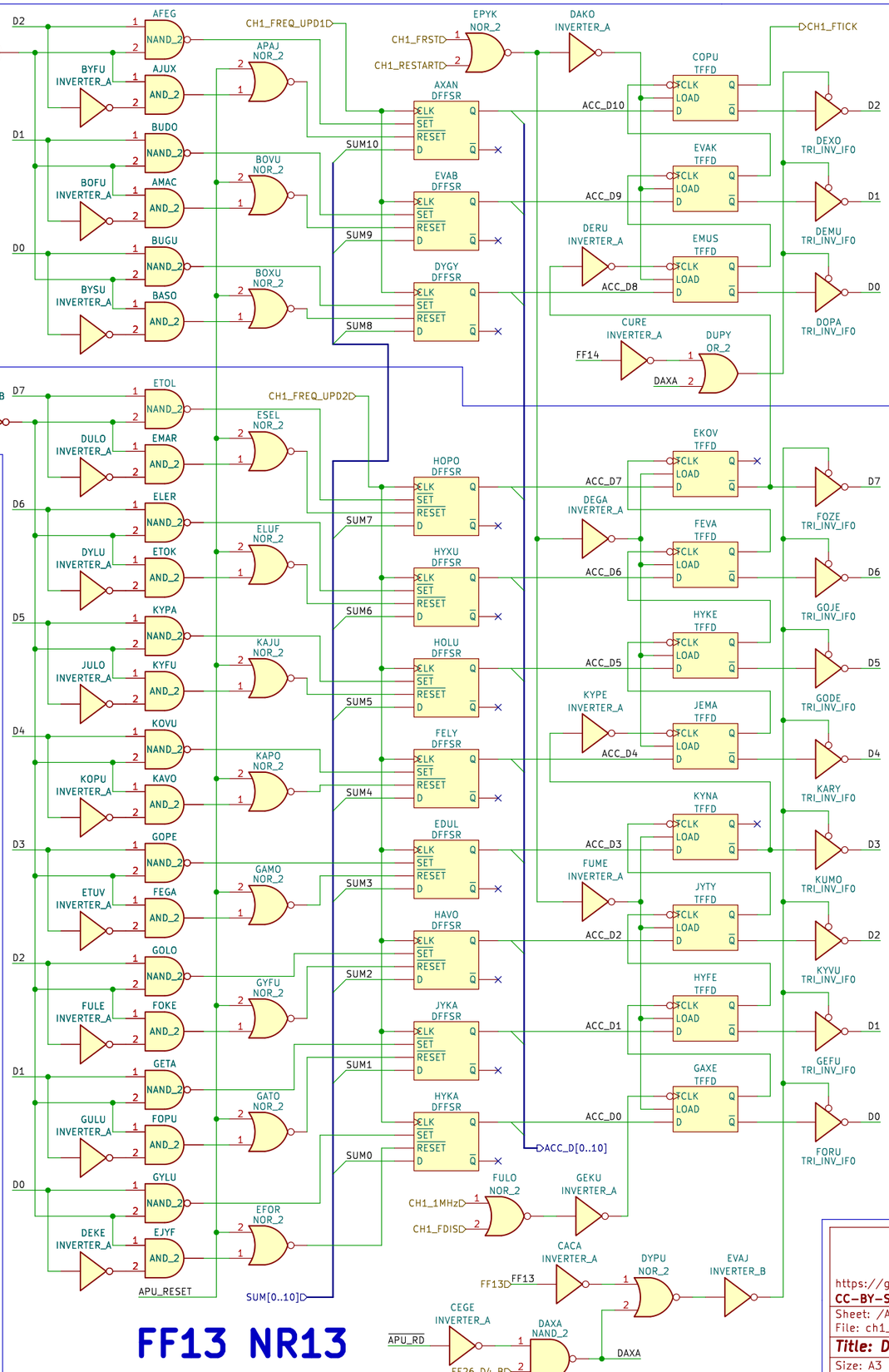
FF14 NR14



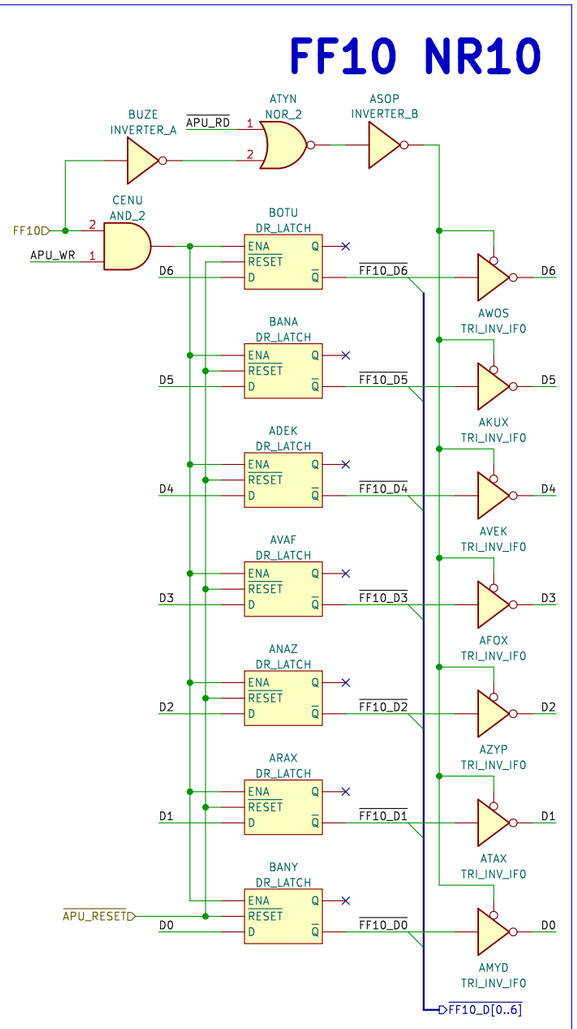
FF12 NR12



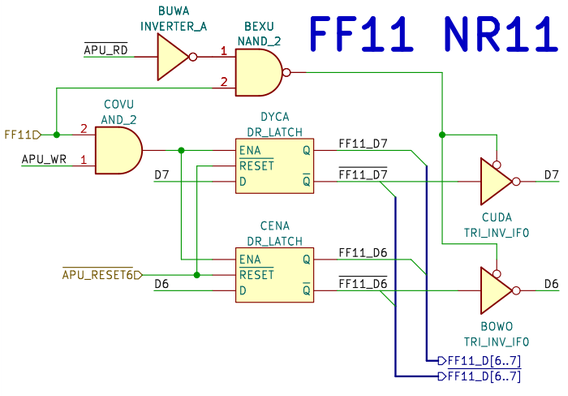
FF13 NR13



FF10 NR10



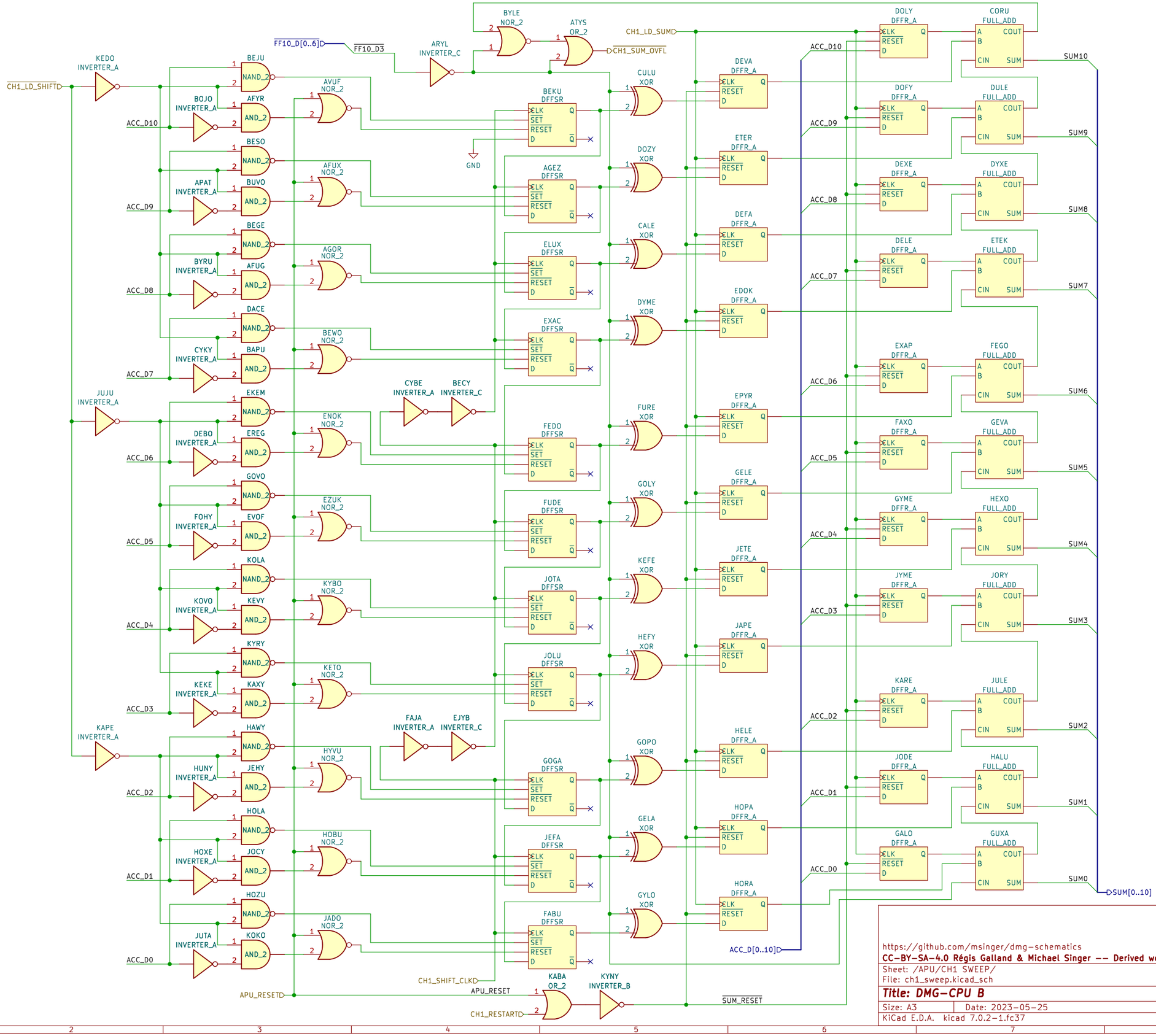
FF11 NR11



Sheet: /APU/CH1 REGS/
File: ch1_regs.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 15/46



https://github.com/msinger/dmg-schematics

Sheet: /APU/CH1 SWEEP/
File: ch1_sweep.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 16/46

Waveform counter

Sweep timer

Duty select

Sweep shift counter

EG timer clocked at 64Hz

Length timer

https://github.com/msinger/dmg-schematics

CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

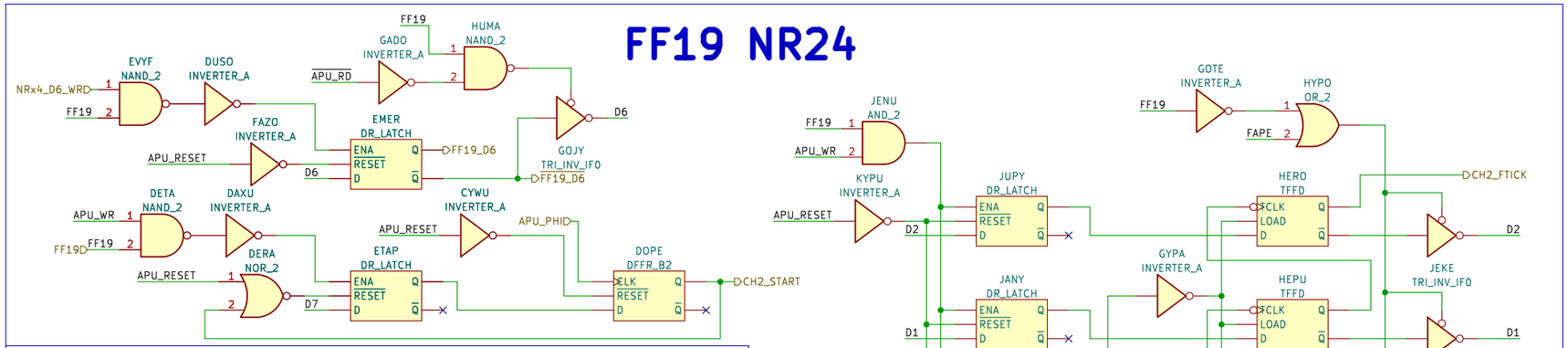
Sheet: /APU/CHANNEL 1/

File: channel1.kicad_sch

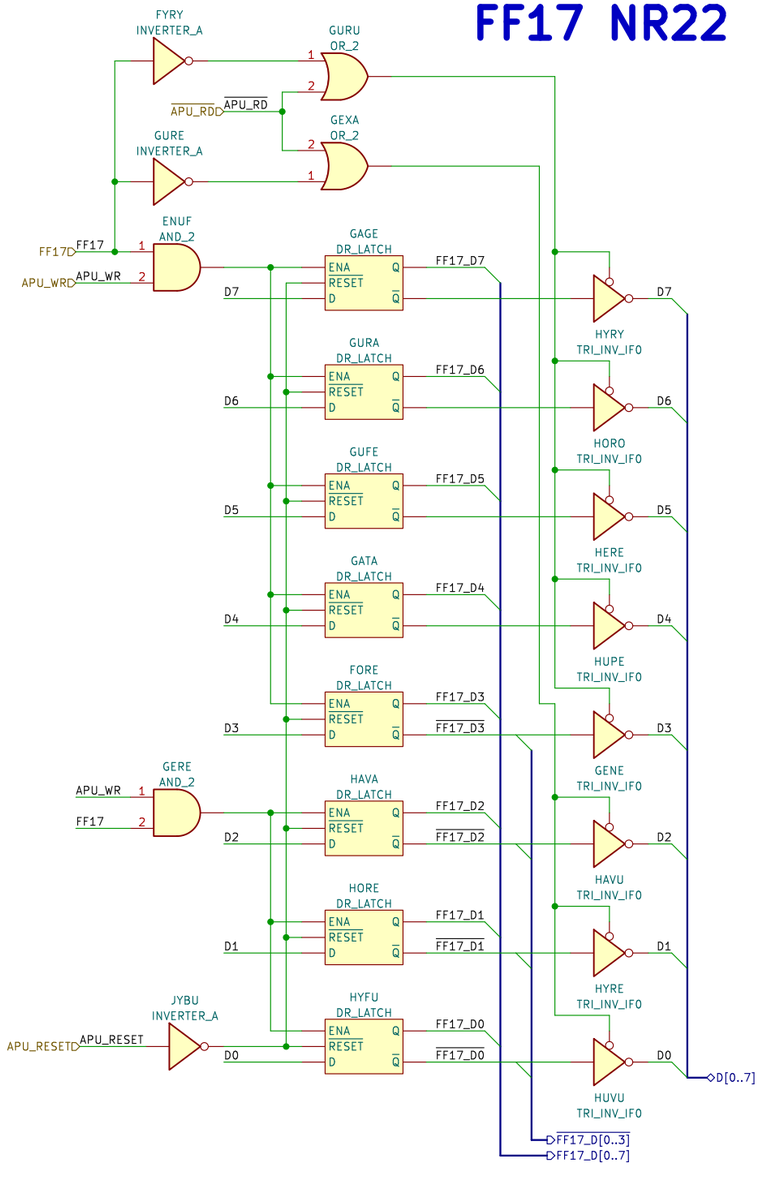
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 17/46

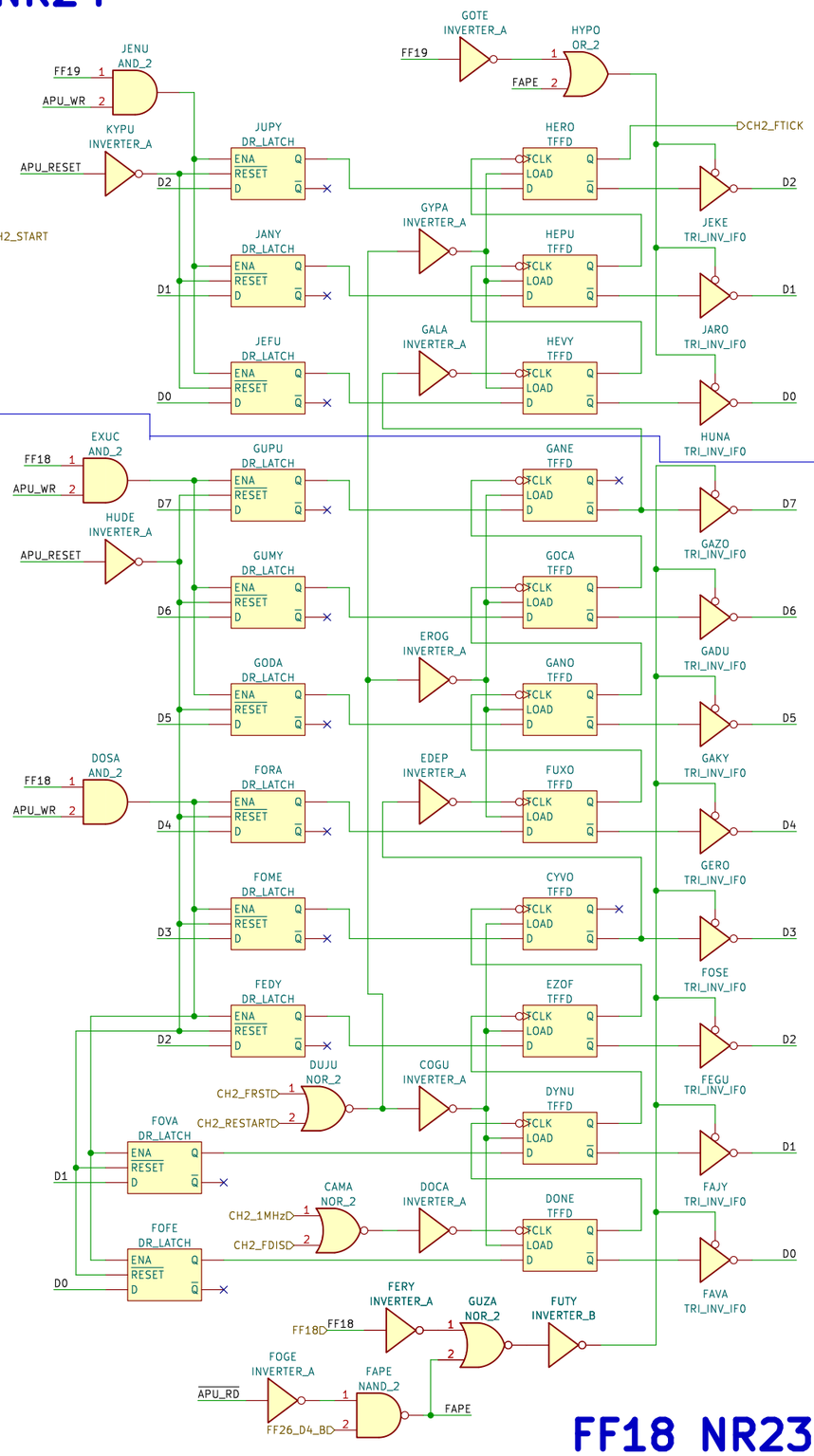
FF19 NR24



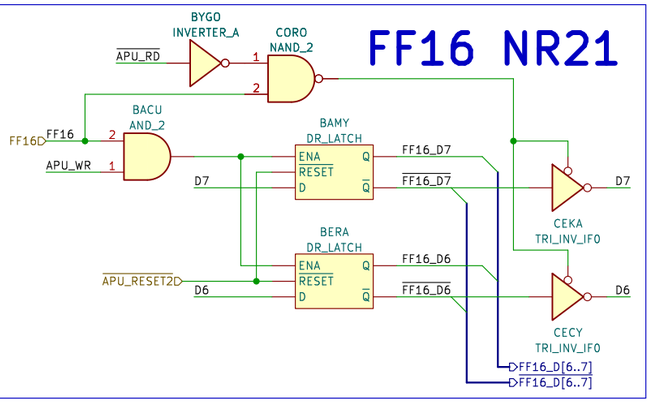
FF17 NR22



FF18 NR23



FF16 NR21



Sheet: /APU/CH2 REGS/		
File: ch2_regs.kicad_sch		
Title: DMG-CPU B		
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 18/46

GALU INVERTER_A
CH2_FTICK
GYRE NOR_3
APU_RESET
CH2_RESTART
GYKO DFFR_B2
CLK RESET D Q Q̄
ETUK INVERTER_A
DAVU INVERTER_A
CH2_FRST
CULE INVERTER_A
Waveform counter
CANO DFFR_B2
DUGE INVERTER_A
FUJY AND_2
CH2_1MHz
CAGY DFFR_B
DYMU AND_2
DYVE DFFR_B
APU_RESET2
EGOG AND_2
DARE INVERTER_A
EXES AO_4
DANE NOR_LATCH
SET RESET Q Q̄
DEFU INVERTER_A
CH2_ACTIVE
CH2_STOP
CYSE AND_2
BONU OR_2
DOME DFFR_B2
FF26_D4_BD
DOMO NOR_2
FF16_D6
FF16_D7
FF16_D[6..7]
DYTA NOR_2
DOJU NOR_2
DOVE NOR_2
FF16_D6
FF16_D7
FF16_D[6..7]
CH2_PWM Duty cycle:
D7-6 = 00 : 00000001 (Q0.Q1.Q2)
D7-6 = 01 : 00000011 (Q1.Q2)
D7-6 = 10 : 00001111 (Q2)
D7-6 = 11 : 11111100 (Q1.Q2)
CH2_RESTART
FOPY AO_2
FF17_D3
FF17_D3
FENA TFFD
CLK LOAD D Q Q̄
FF17_D7
AMOV AND_2
CH2_ENV3
CH2_OUT3
ETUP AO_2
FOMY TFFD
FF17_D6
ASOG AND_2
CH2_ENV2
CH2_OUT2
FARU AO_2
FETE TFFD
FF17_D5
ANYV AND_2
CH2_ENV1
CH2_OUT1
GAFA AO_2
FENO TFFD
FF17_D4
ANAN AND_2
CH2_ENV0
CH2_OUT0
JUPU NOR_3
FF17_D0
FF17_D1
FF17_D2
HOFO OR_3
CH2_EG_STOP
HORU_512Hz
GADE INVERTER_A
HOLY NOR_2
HAFE NOR_4
CH2_RESTART
APU_RESET
JOPA DFFR_B2
HYPA NOR_2
CH2_RESTART
APU_RESET
ERAT NAND_5
CH2_ENV0
CH2_ENV1
CH2_ENV2
CH2_ENV3
FYRE INVERTER_A
GUFY OR_2
HEPO DFFR_B2
JEME NOR_LATCH
EMYR NOR_5
FF17_D[0..3]
JEVY TFFD
KYVO AND_3
FF17_D2
JONA TFFD
FF17_D1
JORE TFFD
FF17_D0
AGET INVERTER_A
AKYD TFFD
D5
BUVA TFFD
D4
BYMO INVERTER_A
CAME TFFD
D3
BUKO INVERTER_A
CONU TFFD
D2
CERA TFFD
D1
ERYC TFFD
D0
HOTA INVERTER_A
BYFE_128Hz
JYNA DFFR_B2
KYLO INVERTER_A
KENE INVERTER_A
KATY INVERTER_A
APU_RESET
HYLY NOR_2
JAKE INVERTER_A
CH2_RESTART
EG timer
DOXA NOR_2
APU_RESET
ELOX DFFR_B2
CH2_1MHz
HYLE OR_2
APU_RESET
CH2_RESTART
CH2_RESTART
CELO INVERTER_A
DALA NOR_LATCH
CH2_START
DORY DFFR_B2
CAZA DFFR_B2
CH2_1MHz
CH2_RESTART
CEXE INVERTER_A
APU_RESET
BODO INVERTER_A
BUTA NAND_LATCH
CH2_FDIS
ARES NOR_2
APU_RESET
CH2_LEN_TIMER_STOP
AGYN NAND_2
APU_WR
FF16
ASYP INVERTER_A
APU_RESET
CH2_RESTART
BENY NOR_3
CYRE DFFR_B2
DEME NOR_3
FF19_D6
BUFY_256Hz
DYRO INVERTER_A
D[0..7]
Length timer
DORA AND_2
FF19_D6
ESYK OR_3
APU_RESET
CH2_STOP
CH2_AMP_EN
FUTE NOR_5
FF17_D3
FF17_D4
FF17_D5
FF17_D6
FF17_D7
FF17_D[0..7]

Sheet: /APU/CHANNEL 2/
File: channel2.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 19/46

FF1A NR30

GEJO AND_2
FF1A
APU_WR
GOVE INVERTER_A
APU_RESET
D7
GUXE DR_LATCH (ENA, RESET, D, Q, Q)
CH3_AMP_EN
FEVO INVERTER_A
FF1A_RDD
FASY NAND_2
FF1A
D7
GEKO TRI_INV_IF0
CH3_AMP_EN
FUVO NOR_2
APU_RESET
FAJU INVERTER_A
GUGU NAND_LATCH (RESET, SET, Q, Q)
CH3_FDIS
CH3_2MHz
FABO INVERTER_A
GYTA DFFR_B2 (CLK, RESET, D, Q, Q)
CH3_RESTART
GYRA DFFR_B2 (CLK, RESET, D, Q, Q)
GAZE INVERTER_A
APU_RESET

FF1E NR34

KOPY INVERTER_A
APU_RESET
HUDA AND_2
FF1E
APU_WR
JACY DR_LATCH (ENA, RESET, D, Q, Q)
JETY DR_LATCH (ENA, RESET, D, Q, Q)
JEMO DR_LATCH (ENA, RESET, D, Q, Q)
D2
D1
D0
GUNU INVERTER_A
FF1E
FUVA OR_2
EGAD
CH3_FTICK
JAPU TFFD (CLK, LOAD, D, Q, Q)
JERA INVERTER_A
KEZA TFFD (CLK, LOAD, D, Q, Q)
KESE INVERTER_A
KEJU TFFD (CLK, LOAD, D, Q, Q)
HUFO TRI_INV_IF0
JURA TRI_INV_IF0
JUVY TRI_INV_IF0
FOVO NAND_2
NRx4_D6_WRD
FF1E
GYGU INVERTER_A
HEKY INVERTER_A
APU_RESET
GORY INVERTER_A
APU_RD
GAWA NAND_2
FF1E
HOTO DR_LATCH (ENA, RESET, D, Q, Q)
FF1E_D6
FF1E_D6
D6
HACA TRI_INV_IF0

FURY NOR_2
APU_RESET
GULO INVERTER_A
GOFY NOR_LATCH (SET, RESET, Q, Q)
GARA DFFR_B2 (CLK, RESET, D, Q, Q)
CH3_RESTART
CH3_RESTART
EPYX NAND_2
APU_WR
FF1E
FENE INVERTER_A
FAKO NOR_2
APU_RESET
GOMA INVERTER_A
APU_RESET
APU_PHID
FOBA DFFR_B2 (CLK, RESET, D, Q, Q)
GAVU DR_LATCH (ENA, RESET, D, Q, Q)
D7

KOTA AND_2
FF1D
APU_WR
KOGU DR_LATCH (ENA, RESET, D, Q, Q)
KANA DR_LATCH (ENA, RESET, D, Q, Q)
JOVE DR_LATCH (ENA, RESET, D, Q, Q)
JYPO DR_LATCH (ENA, RESET, D, Q, Q)
JAFA AND_2
FF1D
APU_WR
JAXA DR_LATCH (ENA, RESET, D, Q, Q)
JOVY DR_LATCH (ENA, RESET, D, Q, Q)
KOGA DR_LATCH (ENA, RESET, D, Q, Q)
D7
D6
D5
D4
D3
D2
D1
D0
KENO TFFD (CLK, LOAD, D, Q, Q)
KAFO TFFD (CLK, LOAD, D, Q, Q)
KEPA TFFD (CLK, LOAD, D, Q, Q)
KYGU TFFD (CLK, LOAD, D, Q, Q)
KEMU TFFD (CLK, LOAD, D, Q, Q)
KUNU TFFD (CLK, LOAD, D, Q, Q)
KUPE TFFD (CLK, LOAD, D, Q, Q)
KUTU TFFD (CLK, LOAD, D, Q, Q)
KASO INVERTER_A
KYRU INVERTER_A
KYKO INVERTER_A
JUTY INVERTER_A
KAMY TRI_INV_IF0
KORA TRI_INV_IF0
JEZA TRI_INV_IF0
JUKE TRI_INV_IF0
JUDE TRI_INV_IF0
KESY TRI_INV_IF0
KAFU TRI_INV_IF0
JOFO TRI_INV_IF0
D[0..7]
HERA NOR_2
CH3_FRST
CH3_RESTART
HEFO NOR_2
CH3_2MHz
CH3_FDIS
KUHA INVERTER_A
APU_RESET
APU_RESET
HOXA INVERTER_A
FF1D
GUTE NOR_2
EGAD
HOVO INVERTER_B
EGAD NAND_2
FF26_D4_BD
DOVO INVERTER_A
APU_RD
APU_RD

FF1C NR32

JOTU INVERTER_A
APU_RD
HENU NAND_2
HAGA AND_2
APU_WR
FF1C
HUKY DR_LATCH (ENA, RESET, D, Q, Q)
FF1C_D6
FF1C_D6
D6
HUCO TRI_INV_IF0
GURO INVERTER_A
APU_RESET
HODY DR_LATCH (ENA, RESET, D, Q, Q)
FF1C_D5
FF1C_D5
D5
HAMU TRI_INV_IF0
FF1C_D[5..6]
FF1C_D[5..6]

EMUT INVERTER_A
D7
FYRU TFFD (CLK, LOAD, D, Q, Q)
FAVE TFFD (CLK, LOAD, D, Q, Q)
FORO TFFD (CLK, LOAD, D, Q, Q)
GEMO TFFD (CLK, LOAD, D, Q, Q)
GAPO TFFD (CLK, LOAD, D, Q, Q)
GATU TFFD (CLK, LOAD, D, Q, Q)
FORY TFFD (CLK, LOAD, D, Q, Q)
GEVO TFFD (CLK, LOAD, D, Q, Q)
D6
D5
D4
D3
D2
D1
D0
GAJY INVERTER_A
FALU INVERTER_A
CH3_LEN_TIMER_STOP
Length timer

FF1B NR31

DERY NAND_2
APU_WR
FF1B
GETO INVERTER_A
GUDA NOR_3
APU_RESET
CH3_RESTART
FEXU DFFR_B2 (CLK, RESET, D, Q)
BUFY_256Hz
FF1E_D6
GEPY NOR_3
GENU INVERTER_A
AJER_2MHz
CALU INVERTER_A
APU_RESET
DAVO DFFR_B2 (CLK, RESET, D, Q)
COKA INVERTER_B
ERED INVERTER_A
CH3_ACTIVE
CH3_ACTIVE
CH3_RESTART
FOZU NOR_LATCH (SET, RESET, Q, Q)
FYGO OR_3
APU_RESET
CH3_AMP_EN
GEDO AND_2
FF1E_D6
EZAS INVERTER_A
DORU INVERTER_A

Sheet: /APU/CH3 REGS/
File: ch3_regs.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 20/46

Test Sample Read

https://github.com/msinger/dmg-schematics

Sheet: /APU/CH3 WAVE RAM/

File: ch3_wave_ram.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 21/46

FF21 NR42

GONY INVERTER_A
HASU OR_2
APU_RD
APU_RD
GOKO AND_2
APU_WR
FF21
FF21D
GEDU DR_LATCH
FF21_D7
D7
D7
HACU TRI_INV_IF0
FEXO INVERTER_A
APU_RESET
GOZO DR_LATCH
FF21_D6
D6
D6
HOGE TRI_INV_IF0
GOKY DR_LATCH
FF21_D5
D5
D5
GODU TRI_INV_IF0
GARU DR_LATCH
FF21_D4
D4
D4
HEDA TRI_INV_IF0
GEKY DR_LATCH
FF21_D3
FF21_D3
D3
D3
GOME TRI_INV_IF0
BOFY INVERTER_A
BOXE OR_2
APU_RD
DACO AND_2
APU_WR
FF21
EZYK DR_LATCH
FF21_D2
FF21_D2
D2
D2
CUZU TRI_INV_IF0
ETYJ DR_LATCH
FF21_D1
FF21_D1
D1
D1
COCE TRI_INV_IF0
EMOK DR_LATCH
FF21_D0
FF21_D0
D0
D0
DEMY TRI_INV_IF0
FF21_D[0..7]
FF21_D[0..3]

FF23 NR44

DULU NAND_2
NRx4_D6_WRD
FF23
CAZO INVERTER_A
CABE INVERTER_A
APU_RESET
APU_RESET
CUNY DR_LATCH
D6
FF23_D6
FF23_D6
BYLO INVERTER_A
APU_RD
FF23
BARE NAND_2
CURY TRI_INV_IF0
D6
CEPY INVERTER_A
FF23_D6
COTE AND_2
CH4_EG_TEST
NOISE_COUNTER_BYPASS
DYRY AND_2
FF26_D4_BD
COMO AND_2
FF23
BAGU NAND_2
COSA INVERTER_A
APU_RD
BEFA INVERTER_A
NOISE_COUNTER_CLK
D0
ATEL TRI_INV_IF0
HAMA_512KHz
GORA DFFR_B2
CH4_RESTART
GATY DFFR_B2
HAPU INVERTER_A
JERY NAND_LATCH
CH4_FDIS
CH4_AMP_EN
HERY NOR_2
APU_RESET
FEBY INVERTER_A
APU_RESET
FALE NOR_2
APU_RESET
GONE DFFR_B2
HAMA_512KHz
CH4_RESTART
CH4_RESTART
HELU INVERTER_A
HAZO NOR_LATCH
FOXE NAND_2
APU_WR
FF23
GOXO INVERTER_A
APU_RESET
GUZY NOR_2
D7
GASO INVERTER_A
APU_RESET
HOGA DR_LATCH
APU_PHI
GYSU DFFR_B2
CH4_START

FF22 NR43

GUGO INVERTER_A
FF22
HEZE OR_2
APU_RD
GAFO DR_LATCH
FF22_D7
D7
D7
HAPY TRI_INV_IF0
GOGO DR_LATCH
FF22_D6
FF22_D6
D6
D6
GAKA TRI_INV_IF0
FYTO DR_LATCH
FF22_D5
FF22_D5
D5
D5
GYPE TRI_INV_IF0
FETA DR_LATCH
FF22_D4
FF22_D4
D4
D4
GEDA TRI_INV_IF0
GETU AND_2
APU_WR
FF22
APU_RESET4
APU_RESET4
KAGE INVERTER_A
APU_RD
JORA NAND_2
FF22
HOSO NAND_2
FF22
APU_WR
KUHU INVERTER_A
HYNE INVERTER_A
APU_RESET
JAMY DR_LATCH
FF22_D3
FF22_D3
D3
D3
KETA TRI_INV_IF0
FF22_D[3..7]
KOKU INVERTER_A
FF22
KEKA OR_2
APU_RD
JAKY DR_LATCH
FF22_D2
FF22_D2
D2
D2
KYRO TRI_INV_IF0
JERO DR_LATCH
FF22_D1
FF22_D1
D1
D1
KAKU TRI_INV_IF0
HUMO AND_2
APU_WR
FF22
APU_RESET5
APU_RESET5
JARE DR_LATCH
FF22_D0
FF22_D0
D0
D0
KAMO TRI_INV_IF0
FF22_D[0..6]
D[0..7]

FF20 NR41

CH4_LEN_TIMER_STOP
CAZE NAND_2
APU_WR
FF20
FURU INVERTER_A
GAPY NOR_3
APU_RESET
CH4_RESTART
FUGO DFFR_B2
BUFY_256Hz
FF23_D6
DODA NOR_3
CUWA INVERTER_A
Length timer
EPEK INVERTER_A
EDOP TFFD
D5
FYLO TFFD
D4
DOTU INVERTER_A
CEDO TFFD
DOPU INVERTER_A
D3
DENA TFFD
D2
FAVY TFFD
D1
DANO TFFD
D0
CH4_RESTART
GENA NOR_LATCH
JUWA INVERTER_A
CH4_ACTIVE
CH4_ACTIVE
EFOT AND_2
FF23_D6
FEGY OR_3
APU_RESET
CH4_AMP_EN
CH4_AMP_EN
GEVY NOR_5
FF21_D3
FF21_D4
FF21_D5
FF21_D6
FF21_D7

Sheet: /APU/CH4 REGS/
File: ch4_regs.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 22/46

FF22_D7-4 = "1101": Noise Counter CLK/16384
FF22_D7-4 = "1100": Noise Counter CLK/8192
FF22_D7-4 = "1011": Noise Counter CLK/4096
FF22_D7-4 = "1010": Noise Counter CLK/2048
FF22_D7-4 = "1001": Noise Counter CLK/1024
FF22_D7-4 = "1000": Noise Counter CLK/512
FF22_D7-4 = "0111": Noise Counter CLK/256
FF22_D7-4 = "0110": Noise Counter CLK/128
FF22_D7-4 = "0101": Noise Counter CLK/64
FF22_D7-4 = "0100": Noise Counter CLK/32
FF22_D7-4 = "0011": Noise Counter CLK/16
FF22_D7-4 = "0010": Noise Counter CLK/8
FF22_D7-4 = "0001": Noise Counter CLK/4
FF22_D7-4 = "0000": Noise Counter CLK/2

Frequency divider:
Noise Counter CLK = 1MHz/ 1, 2, 4, 6, 8, 10, 12 or 14

https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek
Sheet: /APU/CHANNEL 4/
File: channel4.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 23/46

PPU DECODE & VIDEO CONTROL

File: ppu_decode.kicad_sch

CPU_RD
CPU_WR
FEXX
RESET2
PPU_4MHz
A[0..15]
D[0..7]
PPU_HARD_RESET
PPU_RESET
FF46
FF45
FF44
FF41
FF4B
FF4A
FF43
FF42
PPU_WR
PPU_RD
PPU_4MHz
DMA_PHI2
FF40_D[0..7]
FF49
FF48
FF47

FF47–FF49 PALETTES

PPU_RD
PPU_WR
D[0..7]
FF47
FF48
FF49
OBP0_D[0..7]
OBP1_D[0..7]
BGP_D[0..7]

File: palettes.kicad_sch

PIXEL MUX

FF40_D[0..7]
BG_PX_A
BG_PX_B
BGP_D[0..7]
OBP1_D[0..7]
OBP0_D[0..7]
SPRITE_PX_A7
SPRITE_PX_B7
SPRITE_PX_PRIORITY
SPRITE_PX_PALETTE

File: pixel_mux.kicad_sch

FF42–FF43 BACKGROUND SCROLLING

PPU_RD
PPU_WR
D[0..7]
FF42
FF43
PPU_HARD_RESET
FF40_D[0..7]
FF43_D[0..7]
MA[0..12]
H[0..7]
V[0..7]
BP_SEL
BP_CY
TM_CY
IN_WINDOW

File: background.kicad_sch

BG PIXEL SHIFTER

FF40_D[0..7]
MA[0..12]
BP_CY
MD[0..7]
BG_PX_A0
BG_PX_B0
CLKPIPE
LATCH_BG_BP_A
CLK_BG_BP_A
BG_CY_RST

File: bg_px_shifter.kicad_sch

VRAM INTERFACE

D[0..7]
A[0..15]
PPU_HARD_RESET
MD[0..7]
FEXX_FFXX
WRITE
CPU_WR_SYNC
T1T2
CPU_EXT_CS_EN
NON_VRAM_MREQ
TM_BP_CYS
TM_BP_CYS
VRAM_TO_OAM
CPU_VRAM_OAM_RD
TACU
MODE3
SP_BP_CYS
MA[0..12]

File: vram_interface.kicad_sch

FF4A–FF4B WINDOW DETECTION

PPU_RD
PPU_WR
D[0..7]
FF4A
FF4B
PPU_HARD_RESET
PPU_RESET
FF40_D[0..7]
PPU_RESET2
BP_SEL
BP_CY
TM_CY
IN_WINDOW
WX_RST
WX_CLK
WXY_MATCH
MA[0..12]
V[0..7]
H[0..7]
HCLK
INT_VBL

File: win_detect.kicad_sch

BG & WIN CYCLES

PPU_RESET
PPU_4MHz
PPU_RESET2
BP_SEL
BP_CY
TM_CY
IN_WINDOW
WX_RST
WX_CLK
WXY_MATCH
FF40_D[0..7]
FF43_D[0..7]
SH[0..7]
PX9
STOP_MODE3
H_RESET
SPRITE_X_MATCH
MODE3
ATEJ
STOP_OAM_PARSING
BG_CY_RST
CLK_BG_BP_BD
LATCH_BG_BP_AD
CLKPIPED
TM_BP_CYSD
TM_BP_CYSD
LYRYD
TAVED
TOMUD

File: bg_win_cycles.kicad_sch

FEXX_FFXXD
WRITED
CPU_WR_SYNCD
T1T2D
CPU_EXT_CS_END
NON_VRAM_MREQD

FF41 STAT, FF44 LY & FF45 LYC

PPU_RD
PPU_WR
D[0..7]
FF41
FF44
FF45
PPU_HARD_RESET
PPU_4MHz
INT_VBL_BUF
INT_STAT
PX9D
STOP_MODE3D
H_RESETD
STOP_OAM_PARSING
ATEJ
MODE3
SPRITE_X_MATCH
CLKPIPE
MODE2
H[0..7]
H[0..7]
V[0..7]
VCLK2
V_RESET
VCLK
HCLK
INT_VBL

File: ff41_stat.kicad_sch

INT_VBL_BUF
INT_STAT

SPRITE STORE 0–4

OAM_RENDER_A[2..7]
SPRITE_Y_STORE[0..3]
SAVE_SPRITE_NUM[0..9]
SAVE_SPRITE_Y[0..9]
SPRITE_SEL[0..9]

File: sprite_store_part1.kicad_sch

SPRITE STORE 5–9

OAM_RENDER_A[2..7]
SPRITE_Y_STORE[0..3]
SAVE_SPRITE_NUM[0..9]
SAVE_SPRITE_Y[0..9]
SPRITE_SEL[0..9]

File: sprite_store_part2.kicad_sch

SPRITE CONTROL

SAVE_SPRITE_Y[0..9]
SAVE_SPRITE_NUM[0..9]
PPU_RESET
PPU_4MHz
ATEJ
SAVE_SPRITE_X[0..9]
SPRITE_SAVE_EN

File: sprite_control.kicad_sch

SPRITE X PRIORITY

PPU_RESET
SPRITE_SEL[0..9]
FF40_D[0..7]
SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H[0..9]
SPRITE_RST[0..9]
OAM_RENDERING2
ATEJ
SPRITE_X_MATCH
WUTY

File: sprite_x_prio.kicad_sch

SPRITE X MATCHERS 0–4

SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H[0..9]
SPRITE_RST[0..9]
H[0..7]
SPRITE_X[0..7]
SAVE_SPRITE_X[0..9]

File: sprite_x_matchers_part1.kicad_sch

SPRITE X MATCHERS 5–9

SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H[0..9]
SPRITE_RST[0..9]
H[0..7]
SPRITE_X[0..7]
SAVE_SPRITE_X[0..9]

File: sprite_x_matchers_part2.kicad_sch

SPRITE Y COMPARATOR

PPU_RESET
PPU_4MHz
FF40_D[0..7]
SPRITE_Y_STORE[0..3]
V[0..7]
LYRY
TAVE
TOMU
MODE3
SPRITE_Y_MATCH
MA[0..12]
ATEJ
SPRITE_X_MATCH
WUTY
SPRITE_Y_FLIP
TACU
XUJA
TUVO
COTA
OAM_DATA_LATCH
D[0..7]
OAM_B_D[0..7]
OAM_B_RD
SP_BP_CYS
LATCH_SP_BP_AD
LATCH_SP_BP_BD

File: sprite_y_comparator.kicad_sch

SPRITE X MATCH TOP

WUTY
SPRITE_Y_FLIP
CLKPIPE
COTA
OAM_DATA_LATCH
D[0..7]
OAM_A_D[0..7]
OAM_A_RD
SPRITE_X[0..7]
SPRITE_PX_PALETTE
SPRITE_PX_PRIORITY
SPRITE_X_FLIP
SPRITE_ON[0..7]
SPRITE_PX_A[0..7]
SPRITE_PX_B[0..7]

File: sprite_x_match.kicad_sch

SP PIXEL SHIFTER

SPRITE_PX_B[0..7]
SPRITE_PX_A[0..7]
MD[0..7]
SPRITE_ON[0..7]
SPRITE_X_FLIP
SPRITE_PX_B7
SPRITE_PX_A7
CLKPIPE
SP_BP_CYS
LATCH_SP_BP_A
LATCH_SP_BP_B

File: sp_px_shifter.kicad_sch

LCD

PPU_RESET
PPU_4MHz
PPU_4MHz
8192Hz
4096Hz
FF40_D[0..7]
INT_VBL
HCLK
VCLK
V_RESET
VCLK2
V[0..7]
MODE3
ATEJD
STOP_OAM_PARSING
SPRITE_SAVE_END
OAM_RENDERING2
SPRITE_Y_MATCH
XOCE
XUPY
XYSO
OAM_RENDERING
OAM_PARSING
OAM_PARSE_A[2..7]

File: lcd.kicad_sch

8192Hz
4096Hz

OAM

MD[0..7]
OAM_RENDER_A[2..7]
PPU_HARD_RESET
PPU_4MHz
CPU_VRAM_OAM_RD
MODE2
MODE3
TACU
XUJA
TUVO
COTA
OAM_DATA_LATCH
D[0..7]
OAM_B_D[0..7]
OAM_B_RD
XOCE
XUPY
XYSO
OAM_RENDERING
OAM_PARSING
OAM_PARSE_A[2..7]
OAM_A_D[0..7]
OAM_A_RD
PPU_RD
PPU_WR
A[0..15]
CPU_T4
FEXX

File: oam.kicad_sch

FF46 DMA

PPU_RD
PPU_WR
D[0..8]
FF46
PPU_HARD_RESET
DMA_PHI
MA[0..12]
DMA_PHI2
VRAM_TO_OAM
DMA_RUN
DMA_PHI
OAM_ADDR_DMA
DMA_A[0..15]
DMA_ADDR_EXT

File: ff46_dma.kicad_sch

DMA_PHI

CPU_T4
FEXX

OAM_B_D[0..7]
OAM_A_D[0..7]
DMA_A[0..15]
DMA_ADDR_EXT

https://github.com/msinger/dmg-schematics

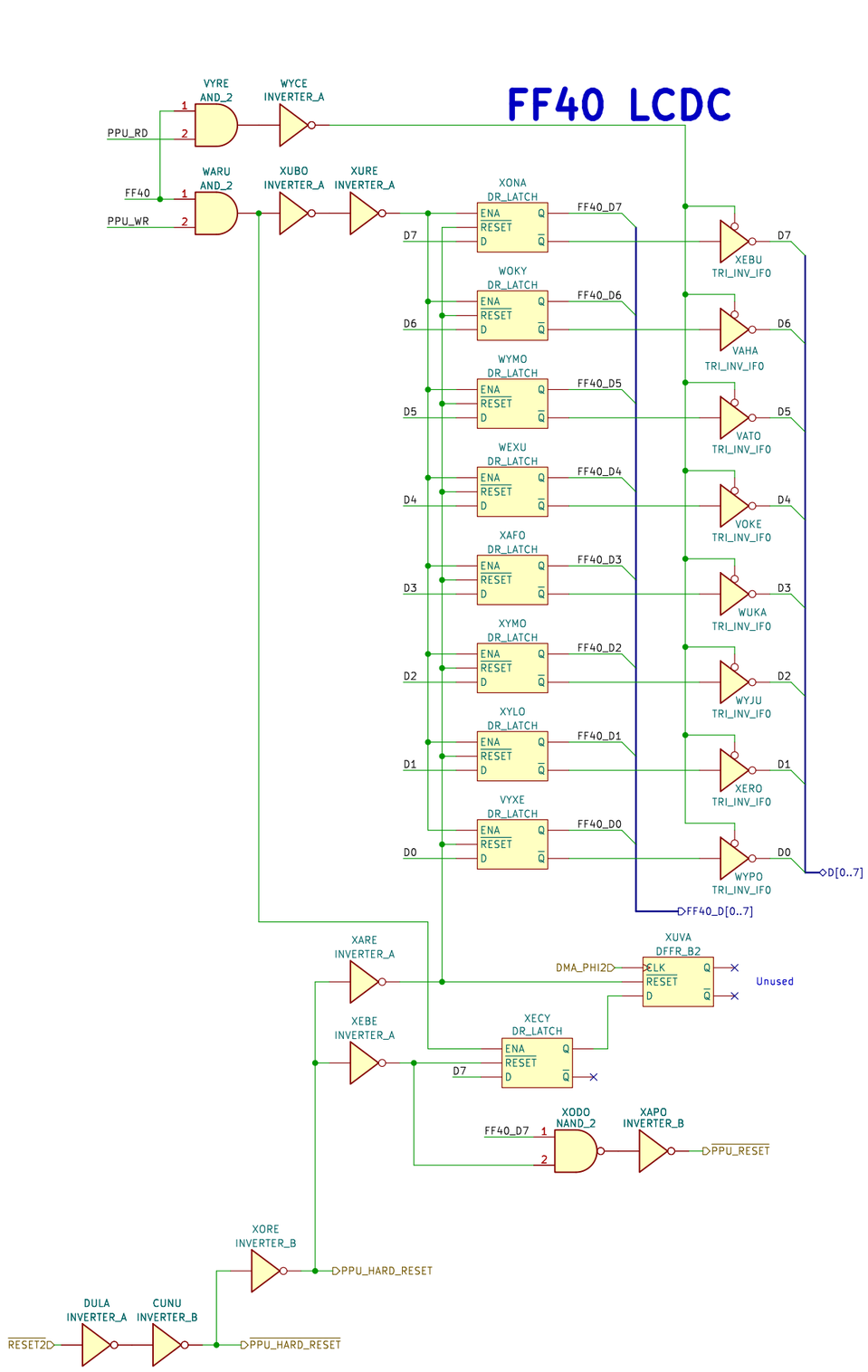
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

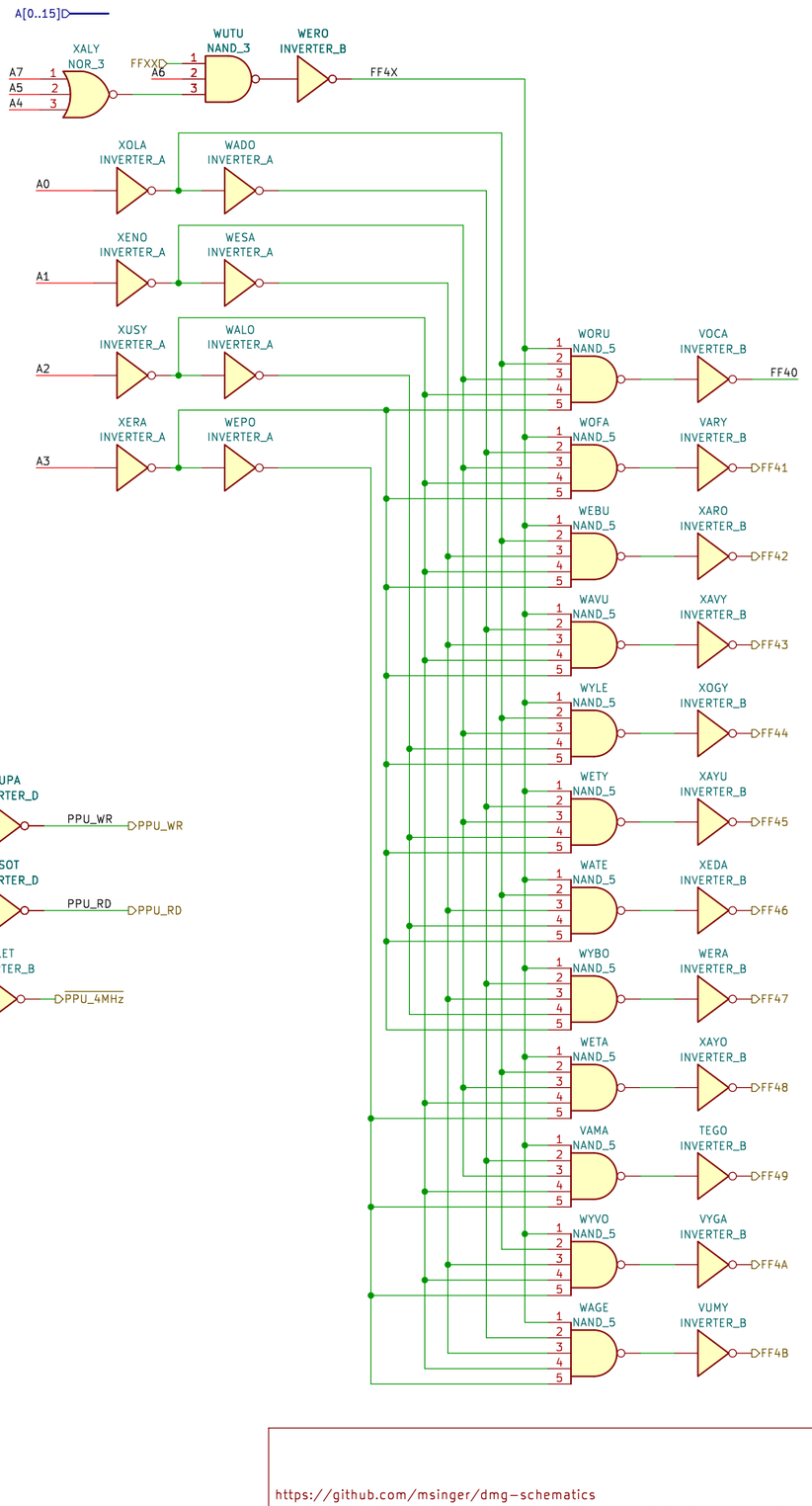
Sheet: /PPU/
File: ppu.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 24/46

FF40 LCDC





https://github.com/msinger/dmg-schematics

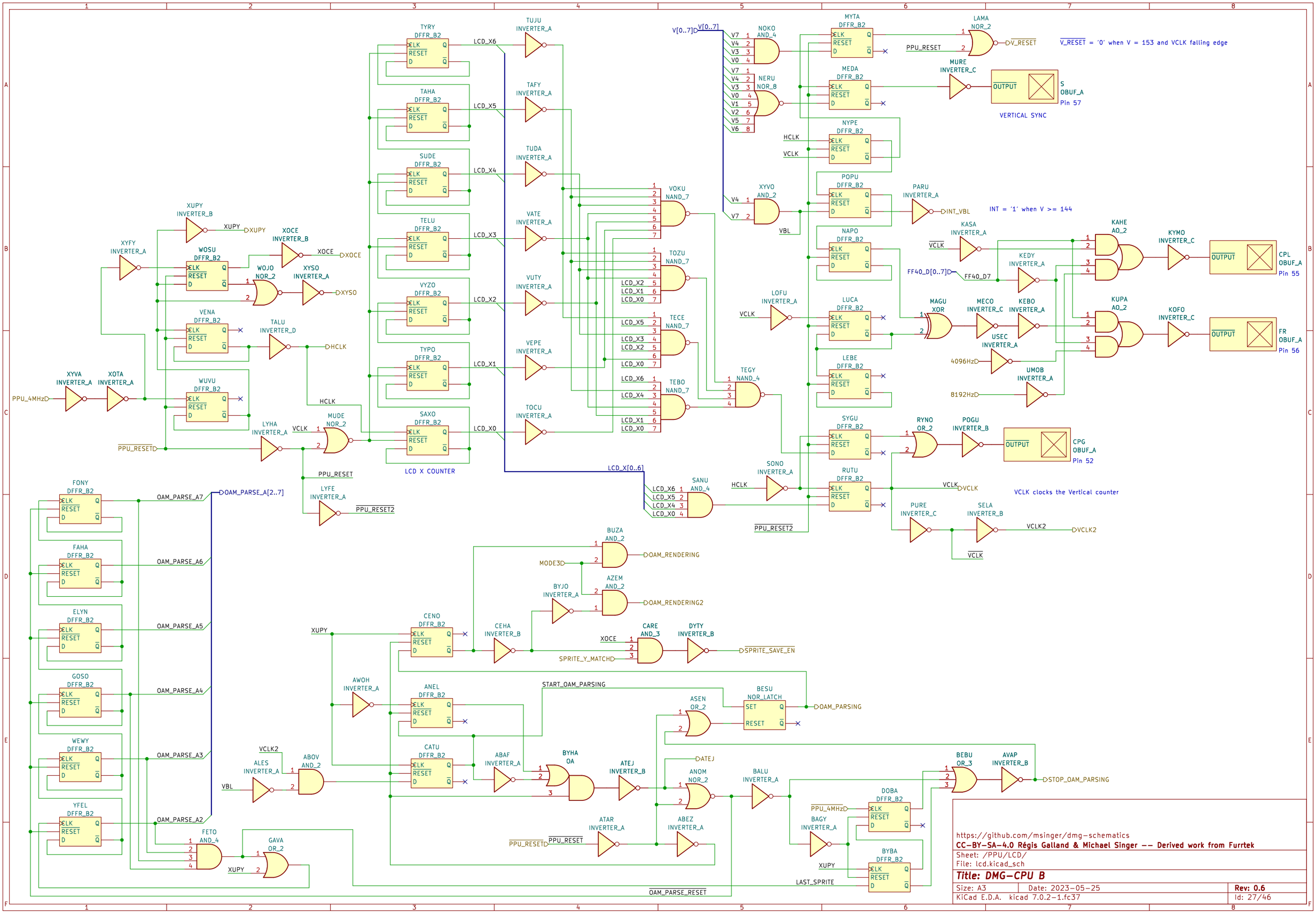
Sheet: /PPU/PPU DECODE & VIDEO CONTROL/
File: ppu_decode.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 25/46

VRAM_TO_OAM
MODE3
XANE NOR_2
XEDU INVERTER_B
MA[0..12]
T1 T1T2D T1T2
SYCY INVERTER_A
SOTO DFFR_B2
CLK RESET D Q Q
TUTO AND_2
RACO INVERTER_A
PPU_HARD_RESET
A[0..15]
TEFA NOR_2
A15
SOSE AND_2
FEXX_FFXX
NON_VRAM_MREQ
VRAM Address range 8000–9FFF
VRAM Externally driven (test mode)
VRAM Internally driven (normal mode)
SOHO AND_2
RAWA INVERTER_A
RACU AND_4
TACUD
SP_BP_CYSD
TM_BP_CYSD
APAM INVERTER_A
VRAM_TO_OAM
RUTE OR_2
RONU INVERTER_B
SEMA AND_2
REFO INVERTER_B
DRV_LOW DRV_HIGH INPUT
MRD IOBUF_A Pin 45
TEGU NAND_2
WRITED
TAVY INVERTER_A
SALE MUX
RUVY INVERTER_A
RYLU NAND_2
SOFY OR_2
RAGU INVERTER_B
TAXY AND_2
SYSY INVERTER_B
MWR IOBUF_A Pin 49
SUDO INVERTER_A
TUJA AND_2
CPU_WR_SYNCD
TYJY MUX
SOHY NAND_2
SEWO OR_2
ROSU INVERTER_B
TODE AND_2
SOKY INVERTER_B
MCS IOBUF_A Pin 43
TEFY INVERTER_A
TUCA AND_2
CPU_EXT_CS_END
TOLE MUX
SERE AND_2
SUTU NOR_4
TM_BP_CYSD
VRAM_TO_OAM
SP_BP_CYSD
ROPY INVERTER_A
MODE3
SAZO AND_2
No VRAM writing during MODE3
REHO INVERTER_A
PONY INVERTER_B
RUMO TRI_INV_IF0
OUTPUT
MA12 OBUF_A Pin 42
RUMA INVERTER_A
PEDU INVERTER_B
RYNA TRI_INV_IF0
MA11 OBUF_A Pin 46
RUKY INVERTER_A
NUVA INVERTER_B
RUSE TRI_INV_IF0
MA10 OBUF_A Pin 44
VODE INVERTER_A
TAGO INVERTER_B
RESE TRI_INV_IF0
MA9 OBUF_A Pin 47
VOVA INVERTER_A
TUJY INVERTER_B
RYSU TRI_INV_IF0
MA8 OBUF_A Pin 48
MUME INVERTER_A
LUBY INVERTER_B
XYBO TRI_INV_IF0
MA7 OBUF_A Pin 41
MEWY INVERTER_A
LEFA INVERTER_B
XOPO TRI_INV_IF0
MA6 OBUF_A Pin 40
MYSA INVERTER_A
LALO INVERTER_B
XOBA TRI_INV_IF0
MA5 OBUF_A Pin 39
MEPA INVERTER_A
LOLY INVERTER_B
XECA TRI_INV_IF0
MA4 OBUF_A Pin 38
MAVU INVERTER_A
LUVO INVERTER_B
XODY TRI_INV_IF0
MA3 OBUF_A Pin 37
MYRE INVERTER_A
LACA INVERTER_B
XYNE TRI_INV_IF0
MA2 OBUF_A Pin 36
MASA INVERTER_A
LOZU INVERTER_B
XUXU TRI_INV_IF0
MA1 OBUF_A Pin 35
MYFU INVERTER_A
LEXE INVERTER_B
XAKY TRI_INV_IF0
MA0 OBUF_A Pin 34
D[0..7]
SUZA TRI_BUF_IF0
TOFA TRI_BUF_IF0
RUJO TRI_BUF_IF0
SEKE TRI_BUF_IF0
SOTE TRI_BUF_IF0
TYGO TRI_BUF_IF0
TEWU TRI_BUF_IF0
TEME TRI_BUF_IF0
MD[0..7]
SAWU OR_2
RADY INVERTER_B
SUKE AND_2
RYZE INVERTER_B
MD7 IOBUF_B Pin 25
RAKU TRI_INV_IF1
SAME INVERTER_A
TOKU TRI_INV_IF1
SEDO OR_2
RYTY INVERTER_B
SAMO AND_2
REKU INVERTER_B
MD6 IOBUF_B Pin 26
RETA TRI_INV_IF1
RABO INVERTER_A
RUPY TRI_INV_IF1
SEJY OR_2
RUMU INVERTER_B
SAZU AND_2
REVU INVERTER_B
MD5 IOBUF_B Pin 27
ROPU TRI_INV_IF1
RORO INVERTER_A
REXU TRI_INV_IF1
SAKO OR_2
RUBE INVERTER_B
SUMO AND_2
RYRO INVERTER_B
MD4 IOBUF_B Pin 28
ROCE TRI_INV_IF1
SANA INVERTER_A
TYJA TRI_INV_IF1
SYBU OR_2
RODU INVERTER_B
SUNA AND_2
RADA INVERTER_B
MD3 IOBUF_B Pin 29
REMO TRI_INV_IF1
RUNO INVERTER_A
RAJU TRI_INV_IF1
ROKO OR_2
RARE INVERTER_B
SEFU AND_2
RAZO INVERTER_B
MD2 IOBUF_B Pin 30
RYDO TRI_INV_IF1
RONA INVERTER_A
RYBU TRI_INV_IF1
SYMA OR_2
RULY INVERTER_B
SOGO AND_2
RYKY INVERTER_B
MD1 IOBUF_B Pin 31
REBA TRI_INV_IF1
RUNA INVERTER_A
ROTA TRI_INV_IF1
SYNU OR_2
RURA INVERTER_B
SEFA AND_2
REGE INVERTER_B
MD0 IOBUF_B Pin 33
RODY TRI_INV_IF1
RERY INVERTER_A
RUGA TRI_INV_IF1
TYVY NAND_2
SEBY INVERTER_A
CPU_VRAM_OAM_RDD
RYJE INVERTER_A
REVO INVERTER_A
ROCY AND_2
RAHU INVERTER_C
ROVE INVERTER_A
RELA OR_2
RENA INVERTER_A
ROFA INVERTER_B

Sheet: /PPU/VRAM INTERFACE/
File: vram_interface.kicad_sch
Title: DMG-CPU B
Size: A3 | Date: 2023-05-25 | Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37 | Id: 26/46


TYRY
DFFR_B2
LCD_X6
TUJU
INVERTER_A
TAHA
LCD_X5
TAFY
SUDE
LCD_X4
TUDA
TELU
LCD_X3
VATE
VYZO
LCD_X2
VUTY
TYPO
LCD_X1
VEPE
SAXO
LCD_X0
TOCU
LCD X COUNTER
LCD_X[0..6]
V[0..7]
NOKO
AND_4
NERU
NOR_8
MYTA
MEDA
NYPE
POPU
NAPO
LUCA
LEBE
SYGU
RUTU
HCLK
VCLK
XYVO
AND_2
VBL
LOFU
PPU_RESET
PPU_RESET2
LAMA
NOR_2
V_RESET
V_RESET = '0' when V = 153 and VCLK falling edge
MURE
OUTPUT
S
OBUF_A
Pin 57
VERTICAL SYNC
PARU
INT_VBL
INT = '1' when V >= 144
KASA
KAHE
AO_2
KYMO
CPL
Pin 55
KEDY
FF40_D[0..7]
FF40_D7
MAGU
XOR
MECO
KEBO
KUPA
KOFO
FR
Pin 56
USEC
4096Hz
8192Hz
UMOB
RYNO
OR_2
POGU
CPG
Pin 52
PURE
SELA
VCLK2
VCLK clocks the Vertical counter
VOKU
NAND_7
TOZU
TECE
TEBO
TEGY
NAND_4
SONO
SANU
AND_4
XUPY
XUPY
XOCE
XOCE
XYFY
WOSU
WOJO
XYSO
VENA
TALU
HCLK
XYVA
XOTA
PPU_4MHz
WUVU
LYHA
MUDE
PPU_RESET
LYFE
PPU_RESET2
FONY
FAHA
ELYN
GOSO
WEWY
YFEL
OAM_PARSE_A7
OAM_PARSE_A6
OAM_PARSE_A5
OAM_PARSE_A4
OAM_PARSE_A3
OAM_PARSE_A2
OAM_PARSE_A[2..7]
FETO
GAVA
BUZA
MODE3
OAM_RENDERING
BYJO
AZEM
OAM_RENDERING2
CENO
CEHA
CARE
DYTY
SPRITE_Y_MATCH
SPRITE_SAVE_EN
AWOH
ANEL
CATU
START_OAM_PARSING
ASEN
BESU
NOR_LATCH
OAM_PARSING
ALES
ABOV
ABAF
BYHA
OA
ATEJ
ANOM
BALU
ATAR
ABEZ
OAM_PARSE_RESET
DOBA
BYBA
BAGY
LAST_SPRITE
BEBU
OR_3
AVAP
STOP_OAM_PARSING
https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek
Sheet: /PPU/LCD/
File: lcd.kicad_sch
Title: DMG-CPU B
Size: A3
Date: 2023-05-25
Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37
Id: 27/46

FF44 LY

FF41 STAT

FF41: WR = PPU INT ENABLE, RD = PPU INT ENABLE + PPU INT
Glitch when writing to this register — All interrupts are enabled before data settles.

FF45 LYC

When all interrupts are enabled,
INT_STAT = '1' when LY = LYC (whole line), VBLANK (MODE1), HBLANK (MODE0),
and Only for a few cycles at the start of OAM parsing when VCLK is high.

STOP MODE3 when H = 167 and no more sprites to fetch

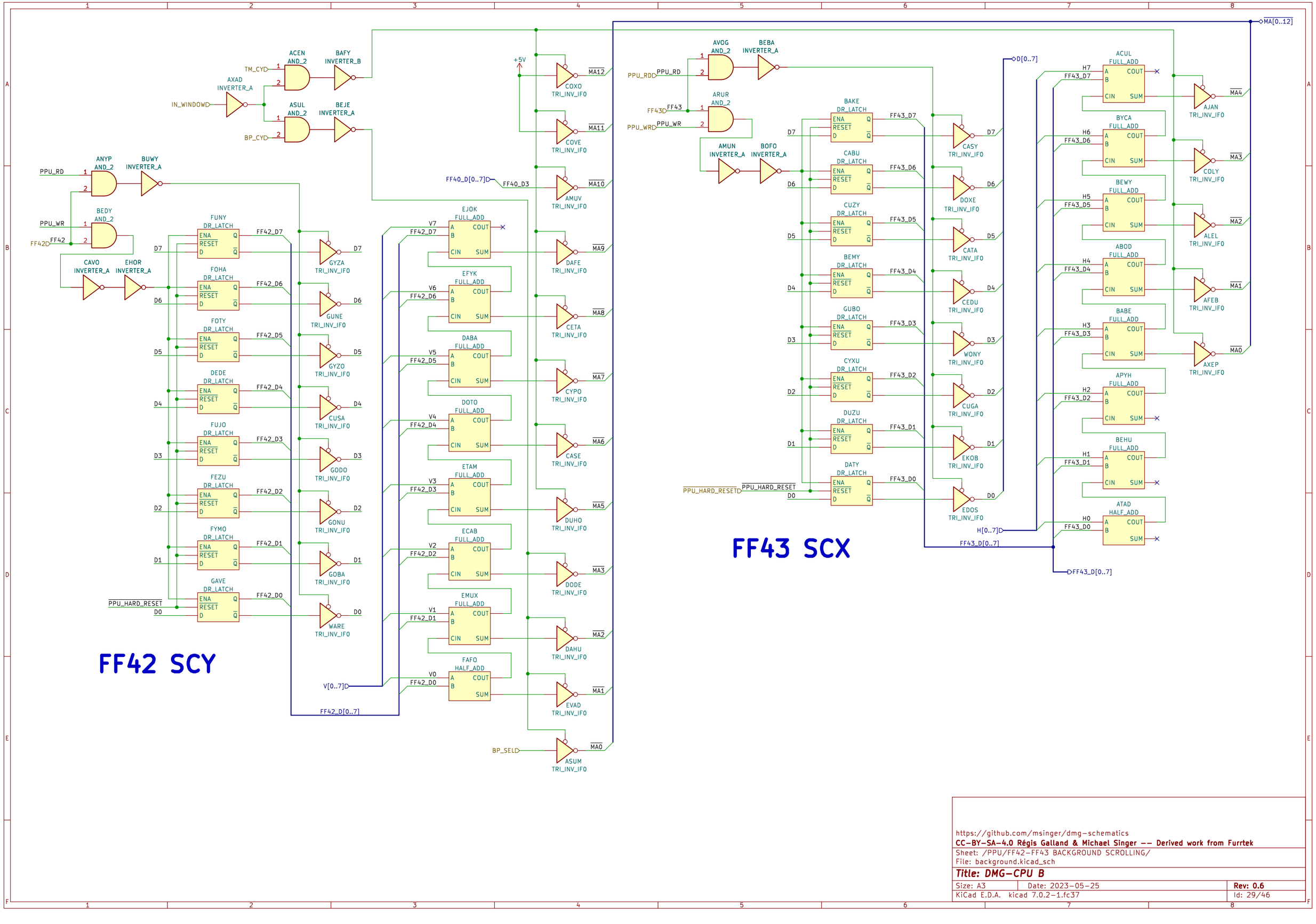
BG/WIN X COUNTER

Y COUNTER

Sheet: /PPU/FF41 STAT, FF44 LY & FF45 LYC/
File: ff41_stat.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 28/46



https://github.com/msinger/dmg-schematics

CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

Sheet: /PPU/FF42-FF43 BACKGROUND SCROLLING/

File: background.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 29/46

FF4A WY

FF4B WX

https://github.com/msinger/dmg-schematics

Sheet: /PPU/FF4A-FF4B WINDOW DETECTION/

File: win_detect.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 30/46

BG/WIN Cycle counter

TAVE resets the cycle counter at cycle 5 only once at the start of a new rendering line.
PORY will reset the counter when Window has started at cycle 5 too.
ROZE will reset the counter at cycle 7 in other cases.

HORIZONTAL SYNC

https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

Sheet: /PPU/BG & WIN CYCLES/
File: bg_win_cycles.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 31/46

CLKPIPED

CLK_BG_BP_B → LESO INVERTER_A → LUVE INVERTER_B → LABU INVERTER_B

BG_CY_RST → BG_CY_RST → LUXA INVERTER_B

+5V

MD7 → PYJU DFFR_A
MD6 → POWY DFFR_A
MD5 → POJU DFFR_A
MD4 → PULO DFFR_A
MD3 → POXA DFFR_A
MD2 → PYZO DFFR_A
MD1 → POZO DFFR_A
MD0 → RAWU DFFR_A
MD[0..7]

BG_TILE7 → RAGA NAND_2 (2) ; SOJA INVERTER_A → RYJY NAND_2 (1)
BG_TILE6 → RAJO NAND_2 (2) ; RAPU INVERTER_A → SUPU NAND_2 (1)
BG_TILE5 → RAJA NAND_2 (2) ; RYLE INVERTER_A → SYWE NAND_2 (1)
BG_TILE4 → RUTO NAND_2 (2) ; RYGA INVERTER_A → SUCA NAND_2 (1)
BG_TILE3 → RYJA NAND_2 (2) ; REVY INVERTER_A → SEBO NAND_2 (1)
BG_TILE2 → RUCE NAND_2 (2) ; TYCE INVERTER_A → SURE NAND_2 (1)
BG_TILE1 → SOLY NAND_2 (2) ; RUCO INVERTER_A → SENO NAND_2 (1)
BG_TILE0 → TUXE NAND_2 (2) ; TOSA INVERTER_A → SEJA NAND_2 (1)

BG_PX_B

SOHU DFFSR (RAGA)
RALU DFFSR (RAJO)
SETU DFFSR (RAJA)
SOBO DFFSR (RUTO)
RYSA DFFSR (RYJA)
SADY DFFSR (RUCE)
TACA DFFSR (SOLY)
TOMY DFFSR (TUXE)

GND

BG_TILE[0..7]

BP_CY

FF40_D[0..7] → FF40_D4 → VUZA NOR_2

BG_TILE7 → VURY TRI_INV_IF1 → MA12
BG_TILE6 → TOBO TRI_INV_IF1 → MA11
BG_TILE5 → SUVO TRI_INV_IF1 → MA10
BG_TILE4 → RESO TRI_INV_IF1 → MA9
BG_TILE3 → ROHA TRI_INV_IF1 → MA8
BG_TILE2 → RUSA TRI_INV_IF1 → MA7
BG_TILE1 → VEJY TRI_INV_IF1 → MA6
BG_TILE0 → SEZU TRI_INV_IF1 → MA5
VAPY TRI_INV_IF1 → MA4

LATCH_BG_BP_A → METE INVERTER_A → LOMA INVERTER_A → LUNA INVERTER_A

MA[0..12]

BG_CY_RST → LOZE INVERTER_B

MD7 → NEFO D_LATCH_A2
MD6 → NASA D_LATCH_A2
MD5 → MYJY D_LATCH_A2
MD4 → MEGU D_LATCH_A2
MD3 → LUZO D_LATCH_A2
MD2 → MUKU D_LATCH_A2
MD1 → NUDU D_LATCH_A2
MD0 → LEGU D_LATCH_A2

NEFO (NAJA) ; NOBO INVERTER_A → NADY NAND_2 (NUTE) ; NEZE INVERTER_A → NYHA NAND_2 (LODO) ; LOXA INVERTER_A → LERU NAND_2 (MYVY) ; LALA INVERTER_A → MOSY NAND_2 (LYDU) ; LOMY INVERTER_A → LUJA NAND_2 (LOTO) ; LEKE INVERTER_A → LUTU NAND_2 (NYXO) ; NOLY INVERTER_A → NEXA NAND_2 (LAKY) ; LUHE INVERTER_A → LOTY NAND_2

BG_PX_A

PYBO DFFSR (NAJA)
NEDA DFFSR (NUTE)
MODU DFFSR (LODO)
NEPO DFFSR (MYVY)
MACU DFFSR (LYDU)
MOJU DFFSR (LUJA)
NOZO DFFSR (LOTO)
MYDE DFFSR (NYXO)

GND

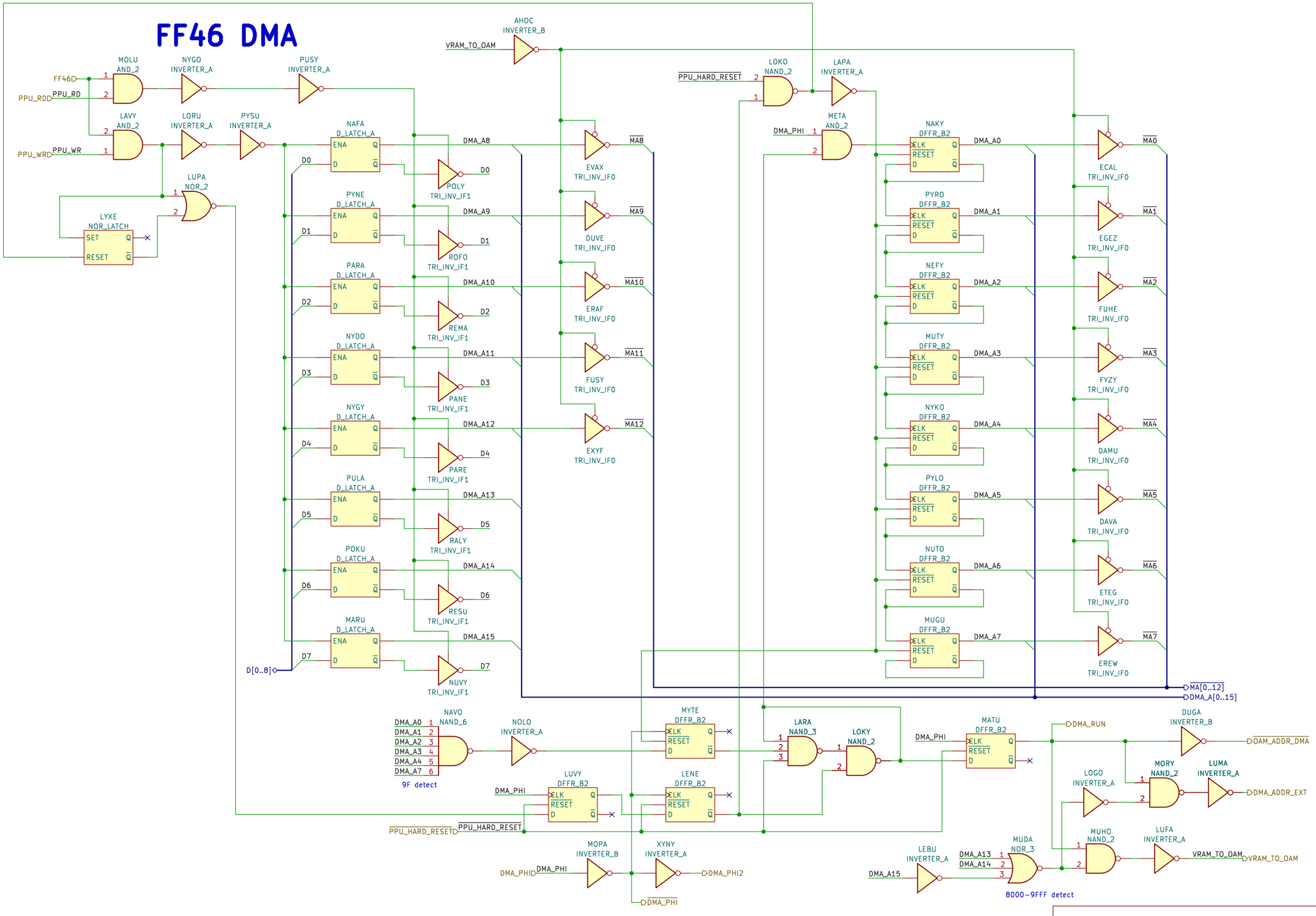
MA bit 3–0 comes from BG or WIN sheets which gives the y offset in the tile

Sheet: /PPU/BG PIXEL SHIFTER/
File: bg_px_shifter.kicad_sch

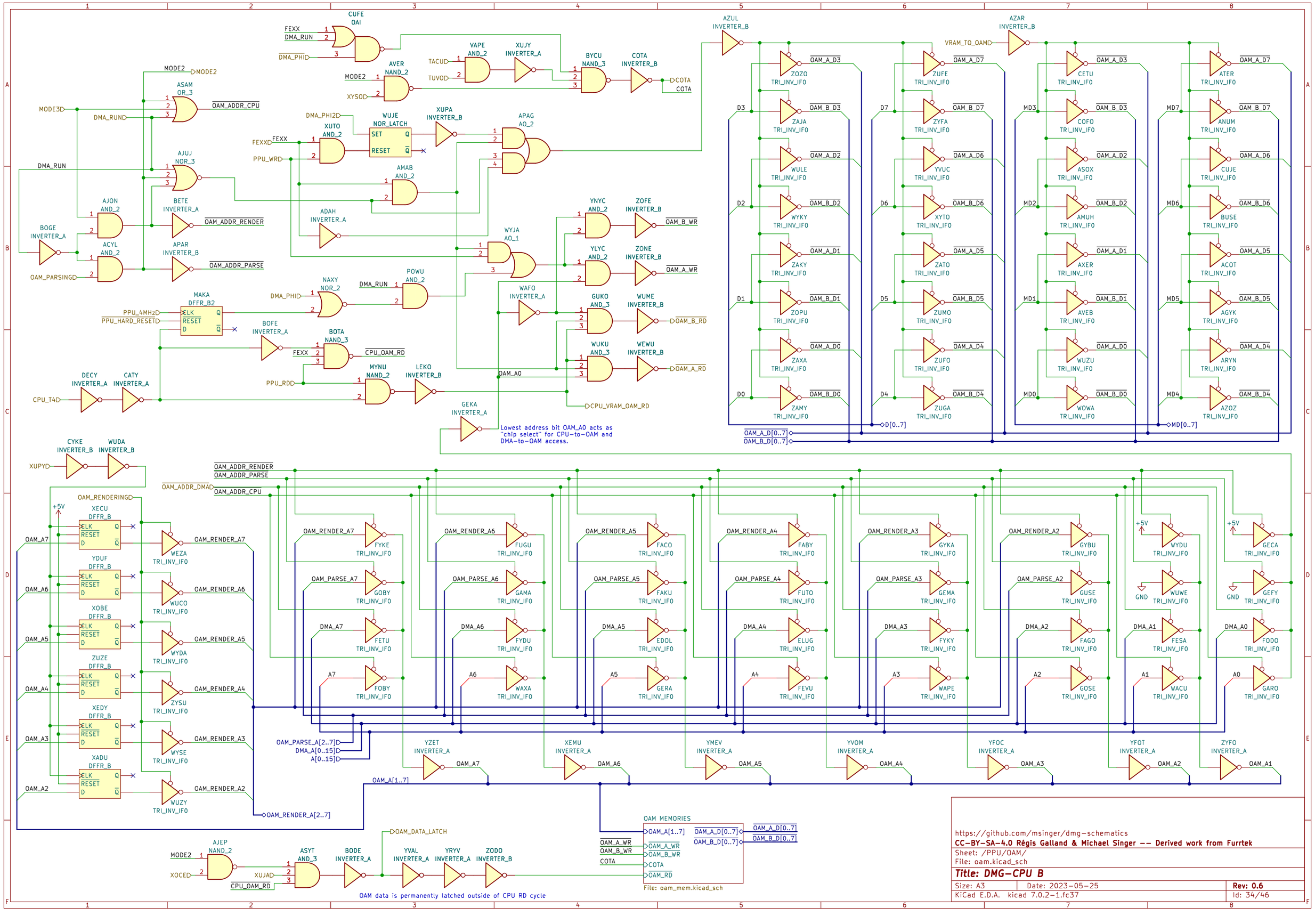
Title: DMG-CPU B

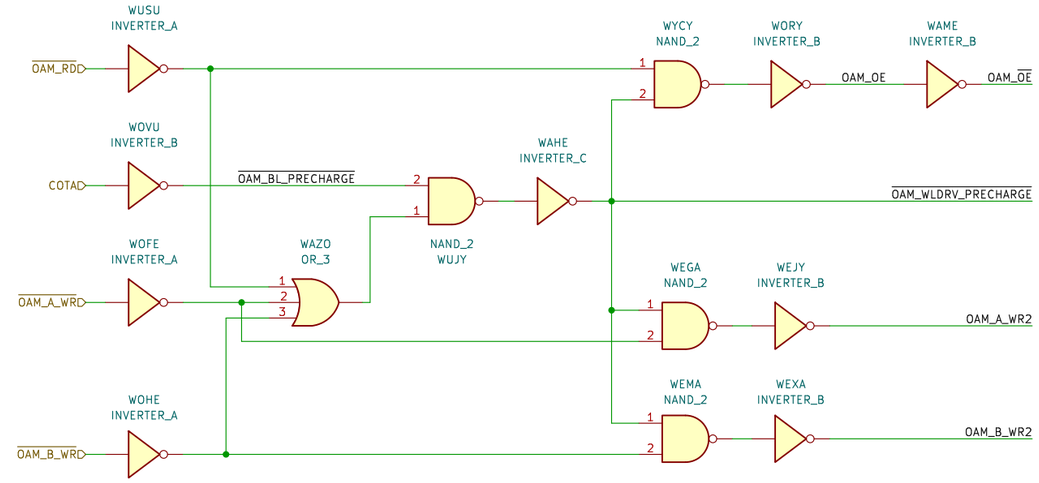
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 32/46

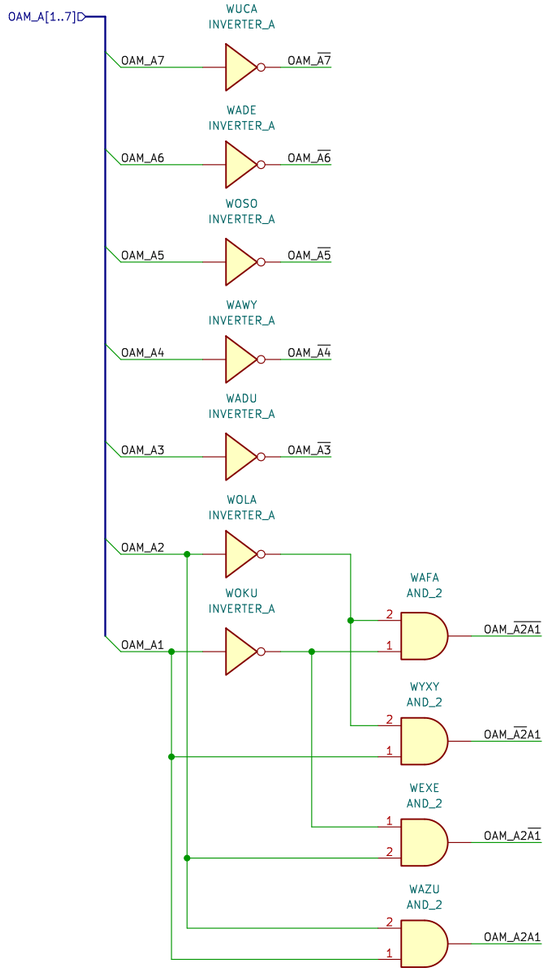
FF46 DMA

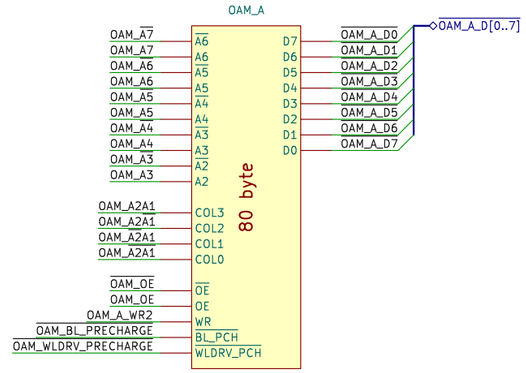


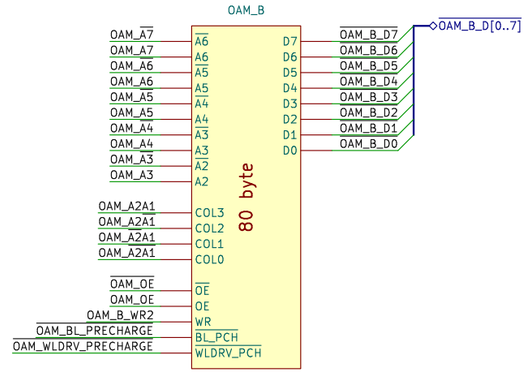
Sheet: /PPU/FF46 DMA/		
File: ff46_dma.kicad_sch		
Title: DMG-CPU B		
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 33/46


CUFE OAI
FEXX
DMA_RUN
DMA_PHID
VAPE AND_2
TACU
TUVO
XUJY INVERTER_A
BYCU NAND_3
COTA INVERTER_B
COTA
AVER NAND_2
MODE2
XYSO
AZUL INVERTER_B
AZAR INVERTER_B
VRAM_TO_OAM
MODE2
ASAM OR_3
MODE3
DMA_RUN
OAM_ADDR_CPU
DMA_PHI2
WUJE NOR_LATCH
SET
RESET
Q
XUPA INVERTER_B
XUTO AND_2
FEXXD
PPU_WR
APAG AO_2
AMAB AND_2
AJUJ NOR_3
AJON AND_2
BETE INVERTER_A
OAM_ADDR_RENDER
BOGE INVERTER_A
ACYL AND_2
APAR INVERTER_B
OAM_ADDR_PARSE
OAM_PARSING
ADAH INVERTER_A
WYJA AO_1
YNYC AND_2
ZOFE INVERTER_B
OAM_B_WR
YLYC AND_2
ZONE INVERTER_B
OAM_A_WR
NAXY NOR_2
DMA_PHID
DMA_RUN
POWU AND_2
MAKA DFFR_B2
CLK
RESET
D
PPU_4MHz
PPU_HARD_RESET
WAFO INVERTER_A
GUKO AND_3
WUME INVERTER_B
OAM_B_RD
BOFE INVERTER_A
BOTA NAND_3
CPU_OAM_RD
WUKU AND_3
WEWU INVERTER_B
OAM_A_RD
DECY INVERTER_A
CATY INVERTER_A
CPU_T4
MYNU NAND_2
LEKO INVERTER_B
PPU_RD
OAM_A0
CPU_VRAM_OAM_RD
GEKA INVERTER_A
Lowest address bit OAM_A0 acts as "chip select" for CPU-to-OAM and DMA-to-OAM access.
ZOZO TRI_INV_IFO
ZAJA TRI_INV_IFO
WULE TRI_INV_IFO
WYKY TRI_INV_IFO
ZAKY TRI_INV_IFO
ZOPU TRI_INV_IFO
ZAXA TRI_INV_IFO
ZAMY TRI_INV_IFO
OAM_A_D3
OAM_B_D3
OAM_A_D2
OAM_B_D2
OAM_A_D1
OAM_B_D1
OAM_A_D0
OAM_B_D0
D3
D2
D1
D0
ZUFE TRI_INV_IFO
ZYFA TRI_INV_IFO
YVUC TRI_INV_IFO
XYTO TRI_INV_IFO
ZATO TRI_INV_IFO
ZUMO TRI_INV_IFO
ZUFO TRI_INV_IFO
ZUGA TRI_INV_IFO
OAM_A_D7
OAM_B_D7
OAM_A_D6
OAM_B_D6
OAM_A_D5
OAM_B_D5
OAM_A_D4
OAM_B_D4
D7
D6
D5
D4
CETU TRI_INV_IFO
COFO TRI_INV_IFO
ASOX TRI_INV_IFO
AMUH TRI_INV_IFO
AXER TRI_INV_IFO
AVEB TRI_INV_IFO
WUZU TRI_INV_IFO
WOWA TRI_INV_IFO
MD3
MD2
MD1
MD0
ATER TRI_INV_IFO
ANUM TRI_INV_IFO
CUJE TRI_INV_IFO
BUSE TRI_INV_IFO
ACOT TRI_INV_IFO
AGYK TRI_INV_IFO
ARYN TRI_INV_IFO
AZOZ TRI_INV_IFO
MD7
MD6
MD5
MD4
D[0..7]
MD[0..7]
OAM_A_D[0..7]
OAM_B_D[0..7]
CYKE INVERTER_B
WUDA INVERTER_B
XUPY
OAM_RENDERING
+5V
XECU DFFR_B
YDUF DFFR_B
XOBE DFFR_B
ZUZE DFFR_B
XEDY DFFR_B
XADU DFFR_B
OAM_A7
OAM_A6
OAM_A5
OAM_A4
OAM_A3
OAM_A2
WEZA TRI_INV_IFO
WUCO TRI_INV_IFO
WYDA TRI_INV_IFO
ZYSU TRI_INV_IFO
WYSE TRI_INV_IFO
WUZY TRI_INV_IFO
OAM_RENDER_A7
OAM_RENDER_A6
OAM_RENDER_A5
OAM_RENDER_A4
OAM_RENDER_A3
OAM_RENDER_A2
OAM_RENDER_A[2..7]
OAM_ADDR_RENDER
OAM_ADDR_PARSE
OAM_ADDR_DMA
OAM_ADDR_CPU
FYKE TRI_INV_IFO
GOBY TRI_INV_IFO
FETU TRI_INV_IFO
FOBY TRI_INV_IFO
FUGU TRI_INV_IFO
GAMA TRI_INV_IFO
FYDU TRI_INV_IFO
WAXA TRI_INV_IFO
FACO TRI_INV_IFO
FAKU TRI_INV_IFO
EDOL TRI_INV_IFO
GERA TRI_INV_IFO
FABY TRI_INV_IFO
FUTO TRI_INV_IFO
ELUG TRI_INV_IFO
FEVU TRI_INV_IFO
GYKA TRI_INV_IFO
GEMA TRI_INV_IFO
FYKY TRI_INV_IFO
WAPE TRI_INV_IFO
GYBU TRI_INV_IFO
GUSE TRI_INV_IFO
FAGO TRI_INV_IFO
GOSE TRI_INV_IFO
WYDU TRI_INV_IFO
WUWE TRI_INV_IFO
FESA TRI_INV_IFO
WACU TRI_INV_IFO
GECA TRI_INV_IFO
GEFY TRI_INV_IFO
FODO TRI_INV_IFO
GARO TRI_INV_IFO
OAM_RENDER_A7
OAM_RENDER_A6
OAM_RENDER_A5
OAM_RENDER_A4
OAM_RENDER_A3
OAM_RENDER_A2
OAM_PARSE_A7
OAM_PARSE_A6
OAM_PARSE_A5
OAM_PARSE_A4
OAM_PARSE_A3
OAM_PARSE_A2
DMA_A7
DMA_A6
DMA_A5
DMA_A4
DMA_A3
DMA_A2
DMA_A1
DMA_A0
A7
A6
A5
A4
A3
A2
A1
A0
OAM_PARSE_A[2..7]
DMA_A[0..15]
A[0..15]
YZET INVERTER_A
XEMU INVERTER_A
YMEV INVERTER_A
YVOM INVERTER_A
YFOC INVERTER_A
YFOT INVERTER_A
ZYFO INVERTER_A
OAM_A7
OAM_A6
OAM_A5
OAM_A4
OAM_A3
OAM_A2
OAM_A1
OAM_A[1..7]
OAM_DATA_LATCH
AJEP NAND_2
MODE2
XOCED
ASYT AND_3
XUJA
CPU_OAM_RD
BODE INVERTER_A
YVAL INVERTER_A
YRYV INVERTER_A
ZODO INVERTER_B
OAM data is permanently latched outside of CPU RD cycle
OAM MEMORIES
OAM_A[1..7]
OAM_A_WR
OAM_B_WR
COTA
OAM_RD
OAM_A_D[0..7]
OAM_B_D[0..7]
File: oam_mem.kicad_sch
https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek
Sheet: /PPU/OAM/
File: oam.kicad_sch
Title: DMG-CPU B
Size: A3
Date: 2023-05-25
Rev: 0.6
KiCad E.D.A. kicad 7.0.2-1.fc37
Id: 34/46









Sheet: /PPU/OAM/OAM MEMORIES/
File: oam_mem.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 35/46

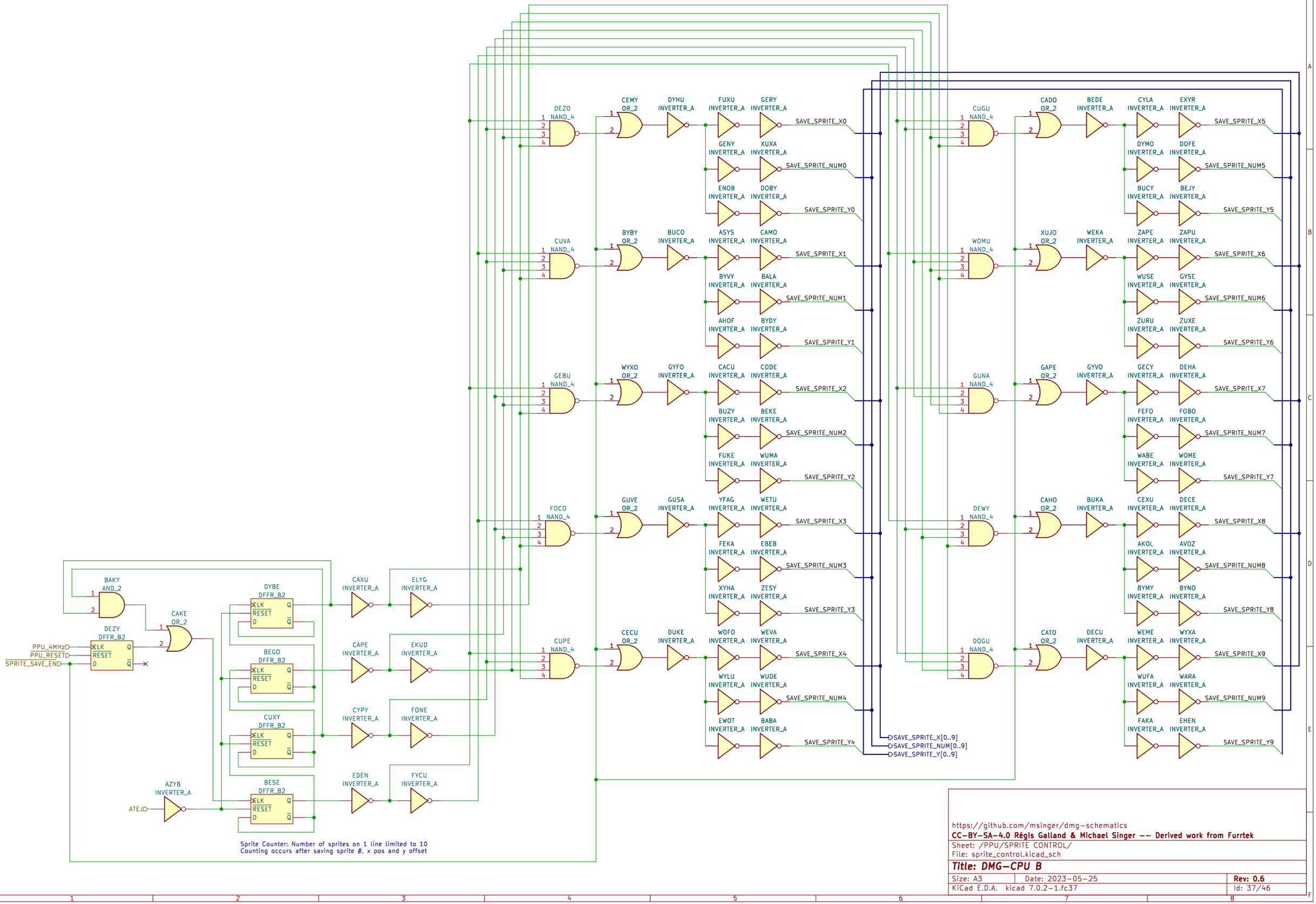
OAM B D[0..7] gives the sprite Y position during parsing and will determine if the sprite appears on the current line.
If it does, D[0..3] gets stored to define the offset in the sprite char.
During rendering, it will contain the Tile address which be used to fecth sprite char data in VRAM.

VONU is 2 CLK5 cycles behind TULY. Sprite bit plane fetching takes 8 cycles during which
TULY = '1' during cycle 2 and 3 and VONU = '1' during cycle 4 and 5.

Sheet: /PPU/SPRITE Y COMPARATOR/
File: sprite_y_comparator.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 36/46



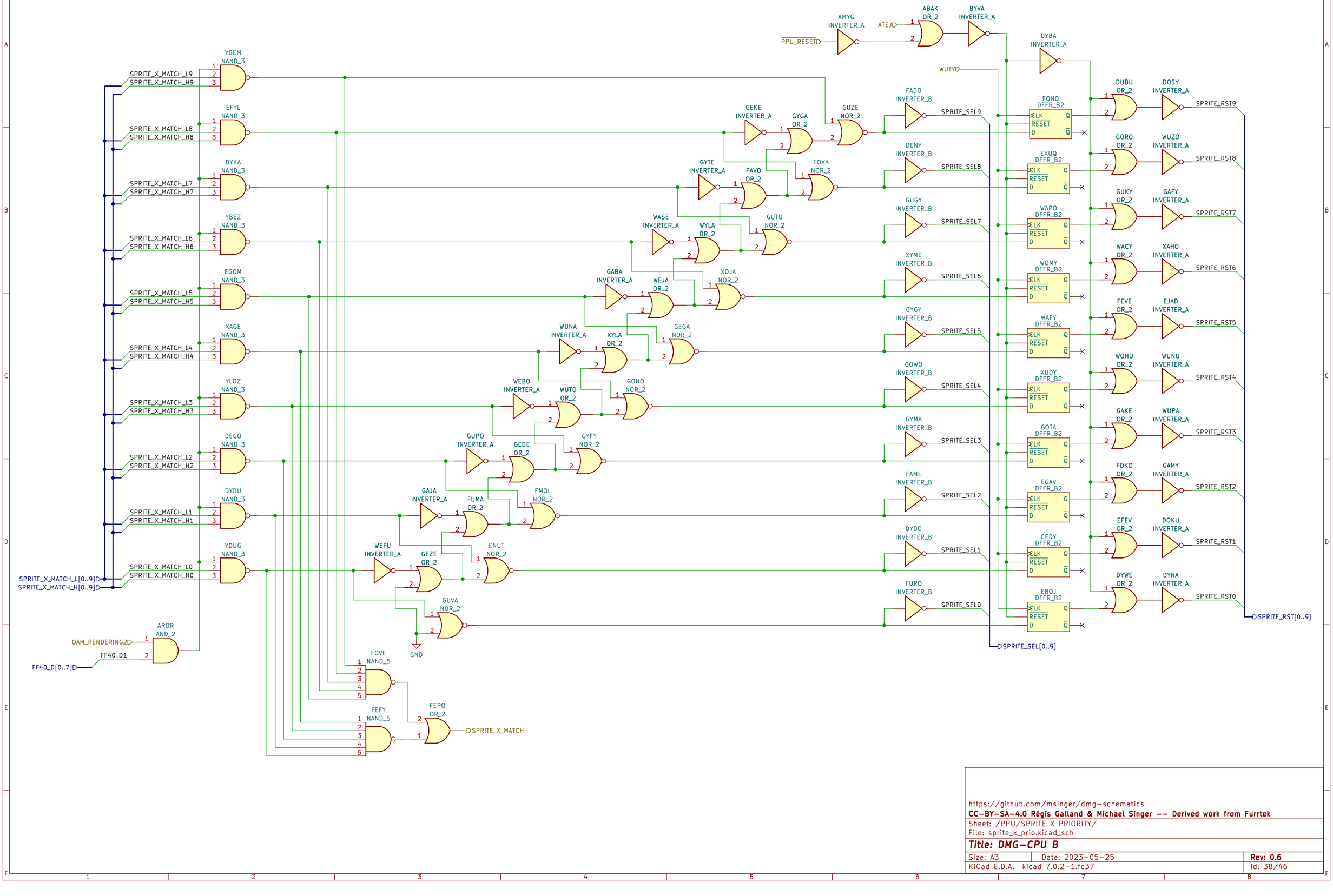
https://github.com/msinger/dmg-schematics

CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

Sheet: /PPU/SPRITE CONTROL/
File: sprite_control.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 37/46



https://github.com/msinger/dmg-schematics

Sheet: /PPU/SPRITE X PRIORITY/
File: sprite_x_prio.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 38/46

SAVE_SPRITE_Y[0..9]
SAVE_SPRITE_NUM[0..9]
SPRITE_SEL[0..9]

SAVE_SPRITE_NUM0
SAVE_SPRITE_Y0
SPRITE_SEL0
ZETU TRI_INV_IF0
ZECE TRI_INV_IF0
ZAVE TRI_INV_IF0
WOKO TRI_INV_IF0
ZUMU TRI_INV_IF0
ZEDY TRI_INV_IF0
WEHE TRI_INV_IF0
AJAL TRI_INV_IF0
BUKY TRI_INV_IF0
GOFO TRI_INV_IF0
YGUS D_LATCH_A
YSOK D_LATCH_A
YZEP D_LATCH_A
WYTE D_LATCH_A
ZONY D_LATCH_A
YWAK D_LATCH_A
GYHO D_LATCH_A
BOZU D_LATCH_A
CUFO D_LATCH_A
FYHY D_LATCH_A

SAVE_SPRITE_NUM1
SAVE_SPRITE_Y1
SPRITE_SEL1
BEMO TRI_INV_IF0
CYBY TRI_INV_IF0
BETY TRI_INV_IF0
CEGY TRI_INV_IF0
CELU TRI_INV_IF0
CUBO TRI_INV_IF0
BEFE TRI_INV_IF0
BACO TRI_INV_IF0
AHUM TRI_INV_IF0
BYRO TRI_INV_IF0
CAJY D_LATCH_A
CUZA D_LATCH_A
COMA D_LATCH_A
CUFA D_LATCH_A
CEBO D_LATCH_A
CADU D_LATCH_A
ABUG D_LATCH_A
ABOP D_LATCH_A
AROF D_LATCH_A
AMES D_LATCH_A

SAVE_SPRITE_NUM2
SAVE_SPRITE_Y2
SPRITE_SEL2
AXEC TRI_INV_IF0
CYRO TRI_INV_IF0
CUVU TRI_INV_IF0
APON TRI_INV_IF0
AFOZ TRI_INV_IF0
CUBE TRI_INV_IF0
ZABY TRI_INV_IF0
WUXE TRI_INV_IF0
WERE TRI_INV_IF0
ZUKE TRI_INV_IF0
BOXA D_LATCH_A
BUNA D_LATCH_A
BULU D_LATCH_A
BECA D_LATCH_A
BYHU D_LATCH_A
BUHE D_LATCH_A
YKUK D_LATCH_A
XAZY D_LATCH_A
XOSY D_LATCH_A
YLOV D_LATCH_A

SAVE_SPRITE_NUM3
SAVE_SPRITE_Y3
SPRITE_SEL3
DEZU TRI_INV_IF0
EFUD TRI_INV_IF0
DONY TRI_INV_IF0
DOWA TRI_INV_IF0
DYGO TRI_INV_IF0
ENAP TRI_INV_IF0
ZYPO TRI_INV_IF0
YJEM TRI_INV_IF0
YWAV TRI_INV_IF0
ZEXE TRI_INV_IF0
DAFU D_LATCH_A
DEBA D_LATCH_A
DUHA D_LATCH_A
DUNY D_LATCH_A
DESE D_LATCH_A
DEVY D_LATCH_A
ZURY D_LATCH_A
ZENE D_LATCH_A
ZYLU D_LATCH_A
ZURO D_LATCH_A

SAVE_SPRITE_NUM4
SAVE_SPRITE_Y4
SPRITE_SEL4
WAJA TRI_INV_IF0
WOXY TRI_INV_IF0
XYRE TRI_INV_IF0
WERU TRI_INV_IF0
WEPY TRI_INV_IF0
WUXU TRI_INV_IF0
BYDO TRI_INV_IF0
BOVE TRI_INV_IF0
BEVY TRI_INV_IF0
BUCE TRI_INV_IF0
XYNU D_LATCH_A
XEGE D_LATCH_A
XABO D_LATCH_A
WANU D_LATCH_A
XEFE D_LATCH_A
XAVE D_LATCH_A
CUMU D_LATCH_A
CONO D_LATCH_A
CAJU D_LATCH_A
CAPO D_LATCH_A

OAM_RENDER_A[2..7]
SPRITE_Y_STORE[0..3]
OAM_RENDER_A7
OAM_RENDER_A6
OAM_RENDER_A5
OAM_RENDER_A4
OAM_RENDER_A3
OAM_RENDER_A2
SPRITE_Y_STORE3
SPRITE_Y_STORE2
SPRITE_Y_STORE1
SPRITE_Y_STORE0

https://github.com/msinger/dmg-schematics
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

Sheet: /PPU/SPRITE STORE 0-4/
File: sprite_store_part1.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 39/46

SAVE_SPRITE_Y[0..9]
SAVE_SPRITE_NUM[0..9]
SPRITE_SEL[0..9]

SAVE_SPRITE_NUM5
SAVE_SPRITE_Y5
SAVE_SPRITE_NUM6
SAVE_SPRITE_Y6
SAVE_SPRITE_NUM7
SAVE_SPRITE_Y7
SAVE_SPRITE_NUM8
SAVE_SPRITE_Y8
SAVE_SPRITE_NUM9
SAVE_SPRITE_Y9

SPRITE_SEL5
SPRITE_SEL6
SPRITE_SEL7
SPRITE_SEL8
SPRITE_SEL9

DALO TRI_INV_IFO
DALY TRI_INV_IFO
DUZA TRI_INV_IFO
WAGA TRI_INV_IFO
DYNY TRI_INV_IFO
DOBO TRI_INV_IFO
AWAT TRI_INV_IFO
BODU TRI_INV_IFO
BUJA TRI_INV_IFO
BACE TRI_INV_IFO

WOCY TRI_INV_IFO
ELYC TRI_INV_IFO
WABO TRI_INV_IFO
EZOC TRI_INV_IFO
WYWY TRI_INV_IFO
WATO TRI_INV_IFO
ZUDO TRI_INV_IFO
ZYTO TRI_INV_IFO
YKOZ TRI_INV_IFO
YBUK TRI_INV_IFO

EVYT TRI_INV_IFO
WABA TRI_INV_IFO
ETAD TRI_INV_IFO
ELEP TRI_INV_IFO
WYGO TRI_INV_IFO
WAKO TRI_INV_IFO
WANA TRI_INV_IFO
WABU TRI_INV_IFO
YPOZ TRI_INV_IFO
WAXE TRI_INV_IFO

ADYB TRI_INV_IFO
APOB TRI_INV_IFO
APYV TRI_INV_IFO
AFEN TRI_INV_IFO
AKYH TRI_INV_IFO
APOC TRI_INV_IFO
BUJY TRI_INV_IFO
AHAC TRI_INV_IFO
BAZU TRI_INV_IFO
BOSO TRI_INV_IFO

YHAL TRI_INV_IFO
YRAD TRI_INV_IFO
XYRA TRI_INV_IFO
YNEV TRI_INV_IFO
ZOJY TRI_INV_IFO
ZARO TRI_INV_IFO
CAWO TRI_INV_IFO
COHO TRI_INV_IFO
GATE TRI_INV_IFO
BYME TRI_INV_IFO

EKAP D_LATCH_A
ETAV D_LATCH_A
EBEX D_LATCH_A
GORU D_LATCH_A
ETYM D_LATCH_A
EKOP D_LATCH_A
ANED D_LATCH_A
ABUX D_LATCH_A
ABEG D_LATCH_A
ACEP D_LATCH_A

GECU D_LATCH_A
FOXY D_LATCH_A
GOHU D_LATCH_A
FOGO D_LATCH_A
GACY D_LATCH_A
GABO D_LATCH_A
ZUBE D_LATCH_A
ZEXO D_LATCH_A
ZAFU D_LATCH_A
ZUMY D_LATCH_A

FUZO D_LATCH_A
GESY D_LATCH_A
FYSU D_LATCH_A
FEFA D_LATCH_A
GYNO D_LATCH_A
GULE D_LATCH_A
XYGO D_LATCH_A
XAKU D_LATCH_A
YGUM D_LATCH_A
XYNA D_LATCH_A

AXUV D_LATCH_A
BADA D_LATCH_A
APEV D_LATCH_A
BADO D_LATCH_A
BEXY D_LATCH_A
BYHE D_LATCH_A
AFYM D_LATCH_A
AFUT D_LATCH_A
AFYX D_LATCH_A
AZAP D_LATCH_A

XUFO D_LATCH_A
XUTE D_LATCH_A
XOTU D_LATCH_A
XYFE D_LATCH_A
YZOR D_LATCH_A
YBER D_LATCH_A
DEWU D_LATCH_A
DYSY D_LATCH_A
FOFO D_LATCH_A
CANA D_LATCH_A

OAM_RENDER_A7
OAM_RENDER_A6
OAM_RENDER_A5
OAM_RENDER_A4
OAM_RENDER_A3
OAM_RENDER_A2
SPRITE_Y_STORE3
SPRITE_Y_STORE2
SPRITE_Y_STORE1
SPRITE_Y_STORE0

OAM_RENDER_A[2..7]
SPRITE_Y_STORE[0..3]

Sheet: /PPU/SPRITE STORE 5-9/
File: sprite_store_part2.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 40/46

SAVE_SPRITE_X0
SPRITE_RST0
SAVE_SPRITE_X1
SPRITE_RST1
SAVE_SPRITE_X2
SPRITE_RST2
SAVE_SPRITE_X3
SPRITE_RST3
SAVE_SPRITE_X4
SPRITE_RST4
SAVE_SPRITE_X[0..9]
SPRITE_RST[0..9]
SPRITE_X[0..7]
H[0..7]
SPRITE_X_MATCH_H[0..9]
SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H0
SPRITE_X_MATCH_H1
SPRITE_X_MATCH_H2
SPRITE_X_MATCH_H3
SPRITE_X_MATCH_H4
SPRITE_X_MATCH_L0
SPRITE_X_MATCH_L1
SPRITE_X_MATCH_L2
SPRITE_X_MATCH_L3
SPRITE_X_MATCH_L4

WELO DR_LATCH
XUNY DR_LATCH
WOTE DR_LATCH
XAKO DR_LATCH
XEPE DR_LATCH
YLAH DR_LATCH
ZOLA DR_LATCH
ZULU DR_LATCH
WOJU XOR
YFUN XOR
WYZA XOR
YPUK XOR
ZOGY XOR
ZEBA XOR
ZAHA XOR
ZOKY XOR
XEBA NOR_4
ZAKO NOR_4

DAKE DR_LATCH
CESO DR_LATCH
DYFU DR_LATCH
CUSY DR_LATCH
DANY DR_LATCH
DUKO DR_LATCH
DESU DR_LATCH
DAZO DR_LATCH
COLA XOR
BOBA XOR
COLU XOR
BAHU XOR
EDYM XOR
EMYB XOR
EBEF XOR
EWOK XOR
CYVY NOR_4
EWAM NOR_4

DUHY DR_LATCH
EJUF DR_LATCH
ENOR DR_LATCH
DEPY DR_LATCH
FOKA DR_LATCH
FYTY DR_LATCH
FUBY DR_LATCH
GOXU DR_LATCH
CEKO XOR
DETY XOR
DOZO XOR
CONY XOR
FUZU XOR
FESO XOR
FOKY XOR
FYVA XOR
CEHU NOR_4
EKES NOR_4

XOMY DR_LATCH
WUHA DR_LATCH
WYNA DR_LATCH
WECO DR_LATCH
XOLY DR_LATCH
XYBA DR_LATCH
XABE DR_LATCH
XEKA DR_LATCH
YVAP XOR
XENY XOR
XAVU XOR
XEVA XOR
YHOK XOR
YCAH XOR
YDAJ XOR
YVUZ XOR
YWOS NOR_4
ZURE NOR_4

YBED DR_LATCH
ZALA DR_LATCH
WYDE DR_LATCH
XEPA DR_LATCH
WEDU DR_LATCH
YGAJ DR_LATCH
ZYJO DR_LATCH
XURY DR_LATCH
ZYKU XOR
ZYPU XOR
XAHA XOR
ZEFE XOR
XEJU XOR
ZATE XOR
ZAKU XOR
YBOX XOR
YKOK NOR_4
YNAZ NOR_4

Sheet: /PPU/SPRITE X MATCHERS 0-4/
File: sprite_x_matchers_part1.kicad_sch

Title: DMG-CPU B

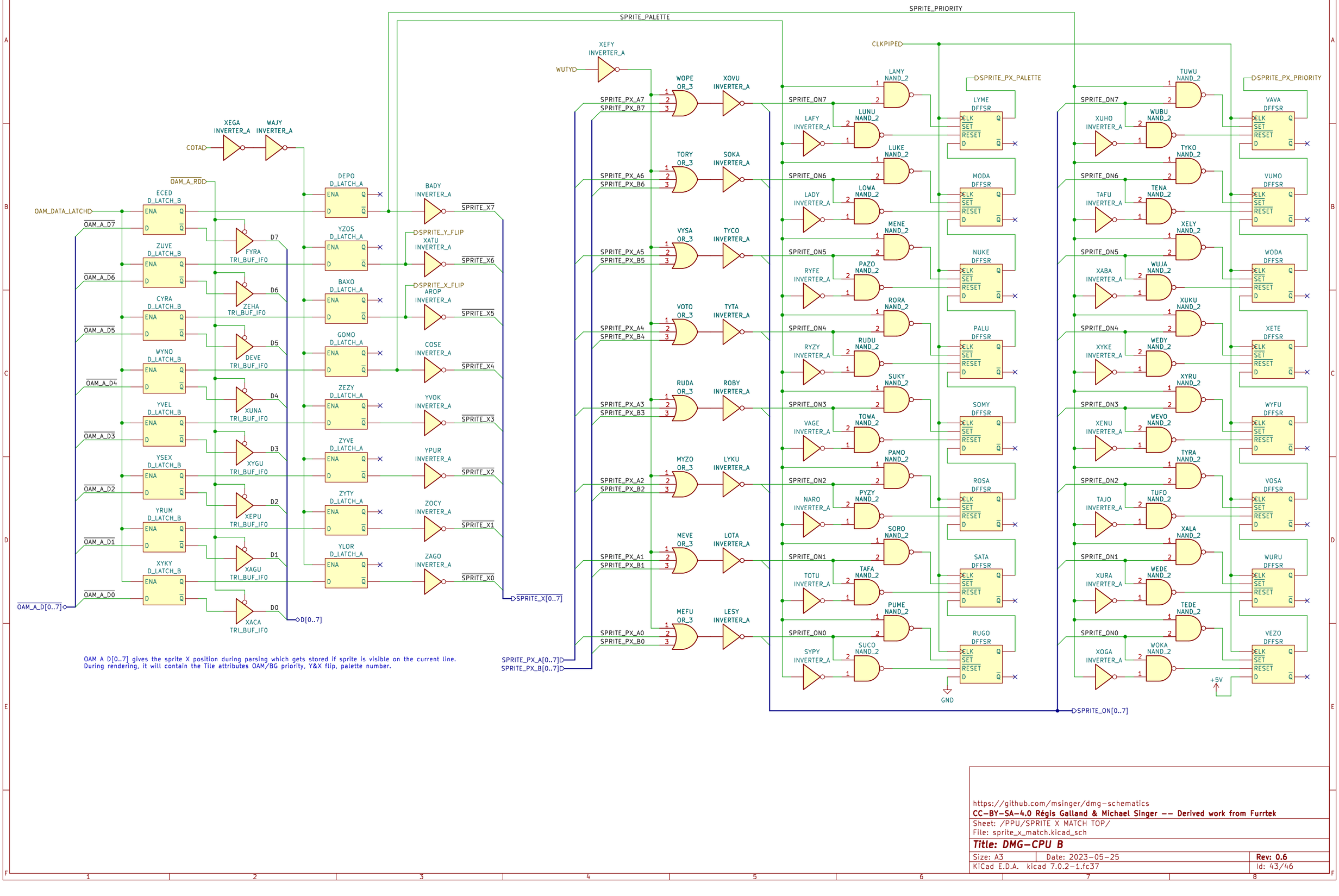
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 41/46

SAVE_SPRITE_X5
SPRITE_RST5
SAVE_SPRITE_X6
SPRITE_RST6
SAVE_SPRITE_X7
SPRITE_RST7
SAVE_SPRITE_X8
SPRITE_RST8
SAVE_SPRITE_X9
SPRITE_RST9
SAVE_SPRITE_X[0..9]
SPRITE_RST[0..9]
SPRITE_X[0..7]
H[0..7]
SPRITE_X_MATCH_H[0..9]
SPRITE_X_MATCH_L[0..9]
SPRITE_X_MATCH_H5
SPRITE_X_MATCH_L5
SPRITE_X_MATCH_H6
SPRITE_X_MATCH_L6
SPRITE_X_MATCH_H7
SPRITE_X_MATCH_L7
SPRITE_X_MATCH_H8
SPRITE_X_MATCH_L8
SPRITE_X_MATCH_H9
SPRITE_X_MATCH_L9
CYWE DR_LATCH
DYBY DR_LATCH
DURY DR_LATCH
CUVY DR_LATCH
FUSA DR_LATCH
FAXA DR_LATCH
FOZY DR_LATCH
FESY DR_LATCH
BAZY XOR
CYLE XOR
CEVA XOR
BUMY XOR
GUZO XOR
GOLA XOR
GEVE XOR
GUDE XOR
COGY NOR_4
FYMA NOR_4
ZECU DR_LATCH
ZOGO DR_LATCH
ZOLY DR_LATCH
ZESA DR_LATCH
YCOL DR_LATCH
YRAC DR_LATCH
YMEM DR_LATCH
YVAG DR_LATCH
ZYGO XOR
ZEMU XOR
ZARE XOR
ZUZY XOR
XOSU XOR
ZUVU XOR
XUCO XOR
ZULO XOR
YWAP NOR_4
YDOT NOR_4
FAZU DR_LATCH
FAXE DR_LATCH
EXUK DR_LATCH
FEDE DR_LATCH
ERAZ DR_LATCH
EPUM DR_LATCH
EROL DR_LATCH
EHYN DR_LATCH
EJOT XOR
ESAJ XOR
DUCU XOR
EWUD XOR
DUSE XOR
DAGU XOR
DYZE XOR
DESO XOR
DAJE NOR_4
CYCO NOR_4
EZUF DR_LATCH
ENAD DR_LATCH
EBOW DR_LATCH
FYCA DR_LATCH
GAVY DR_LATCH
GYPU DR_LATCH
GADY DR_LATCH
GAZA DR_LATCH
DUZE XOR
DAGA XOR
DAWU XOR
EJAW XOR
GOHO XOR
GASU XOR
GABU XOR
GAFE XOR
DAMA NOR_4
FEHA NOR_4
YPOD DR_LATCH
YROP DR_LATCH
YNEP DR_LATCH
YZOF DR_LATCH
XUVY DR_LATCH
XERE DR_LATCH
XUZO DR_LATCH
XEXA DR_LATCH
ZYWU XOR
ZUZA XOR
ZEJO XOR
ZEDA XOR
YMAM XOR
YTYP XOR
YFOP XOR
YVAC XOR
YTUB NOR_4
YLEV NOR_4

Sheet: /PPU/SPRITE X MATCHERS 5-9/
File: sprite_x_matchers_part2.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 42/46

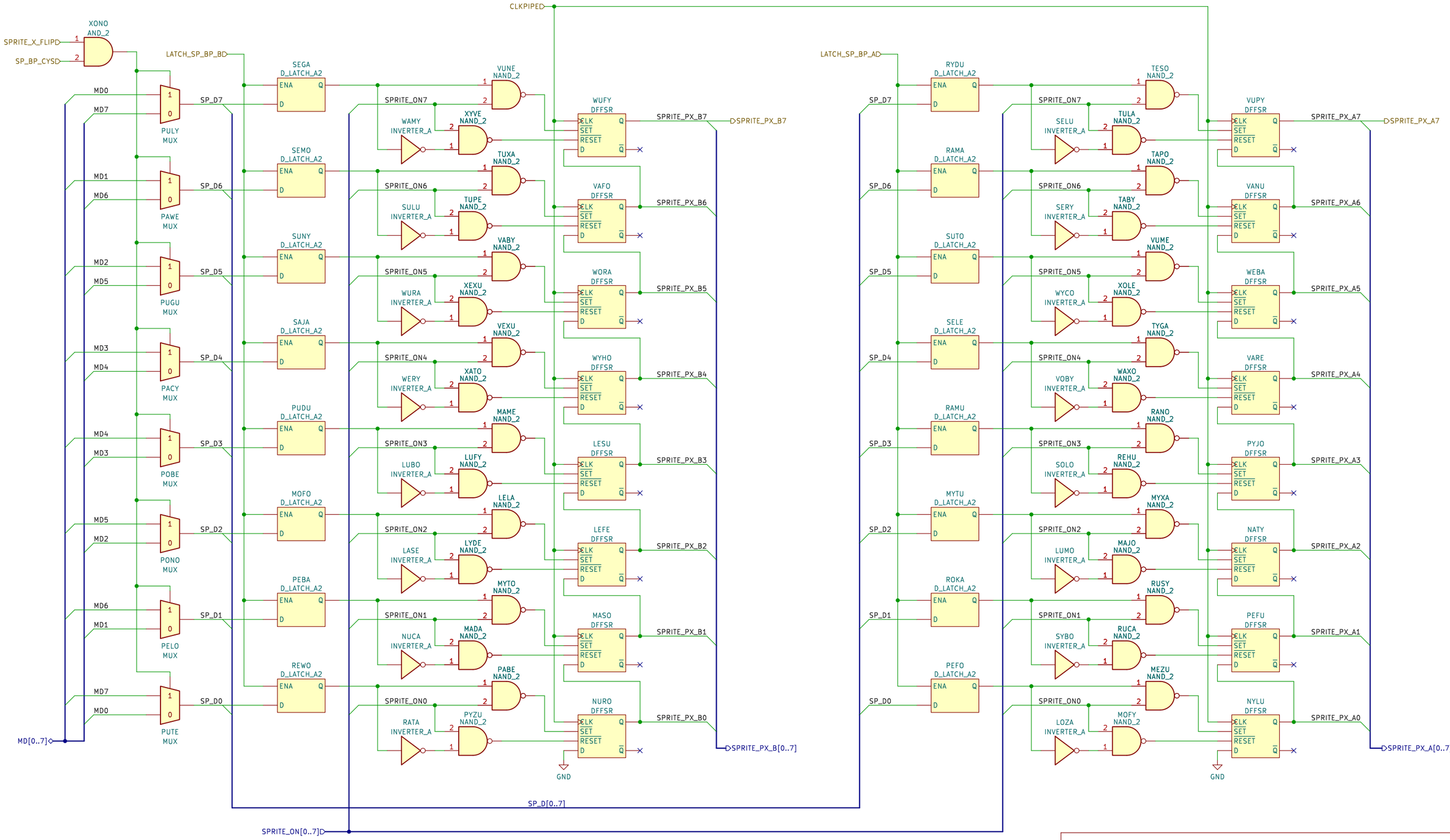


https://github.com/msinger/dmg-schematics

Sheet: /PPU/SPRITE X MATCH TOP/
File: sprite_x_match.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 43/46



https://github.com/msinger/dmg-schematics

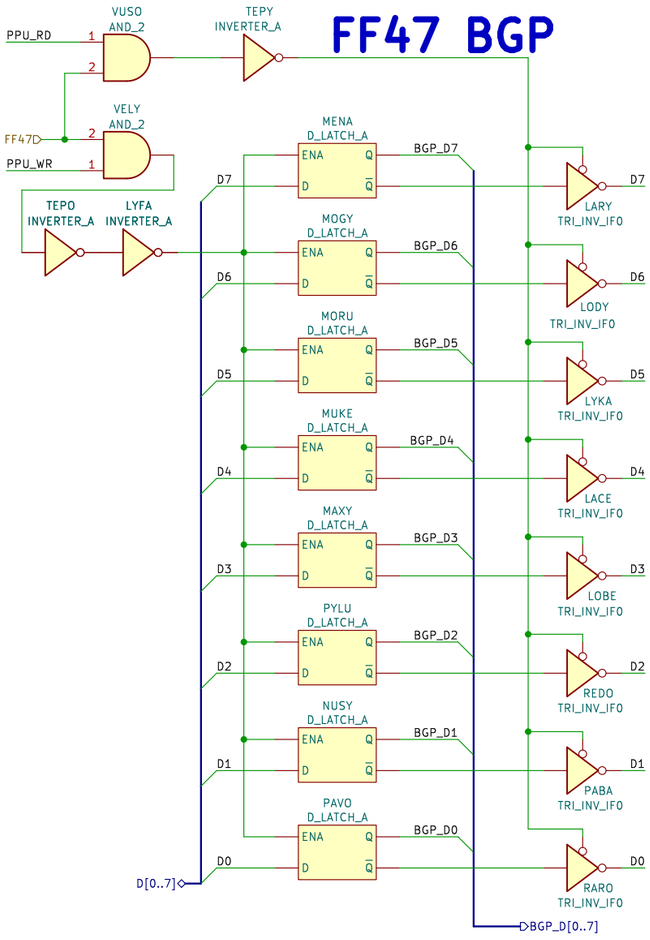
CC-BY-SA-4.0 Régis Galland & Michael Singer -- Derived work from Furrtek

Sheet: /PPU/SP PIXEL SHIFTER/
File: sp_px_shifter.kicad_sch

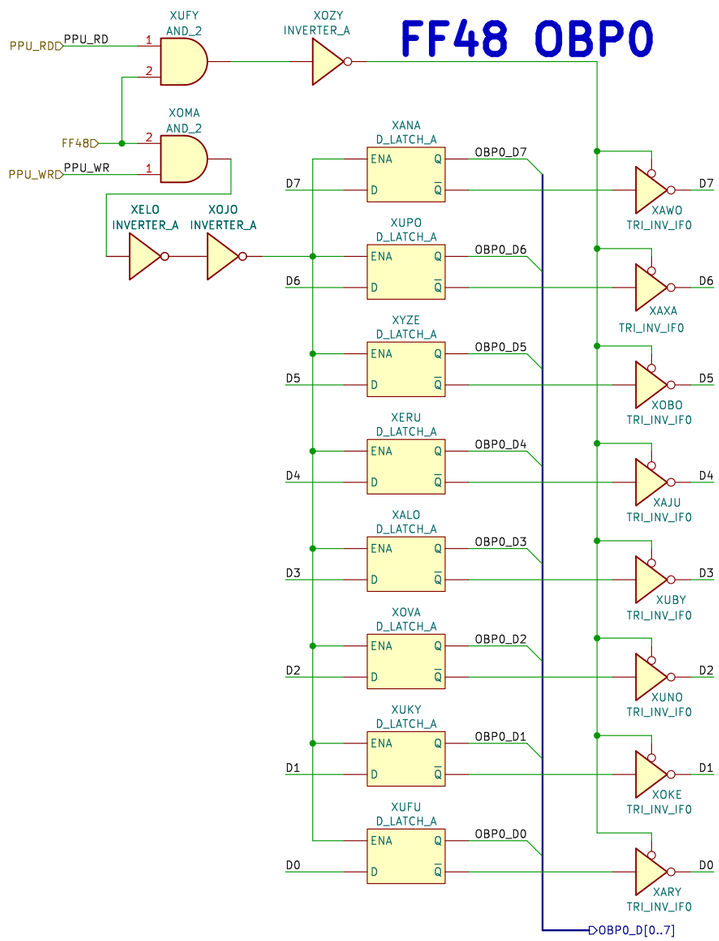
Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 44/46

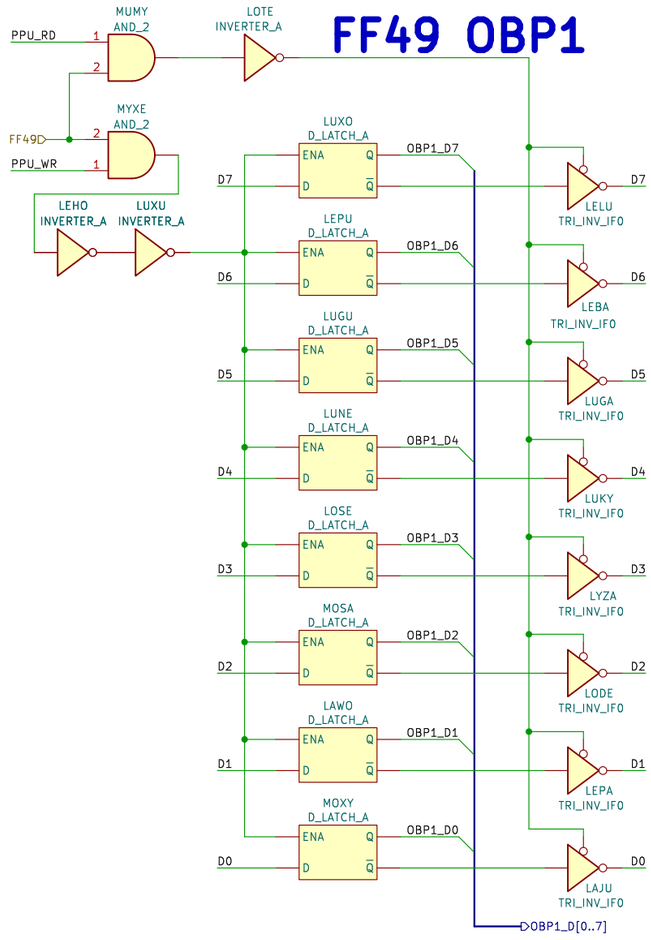
FF47 BGP



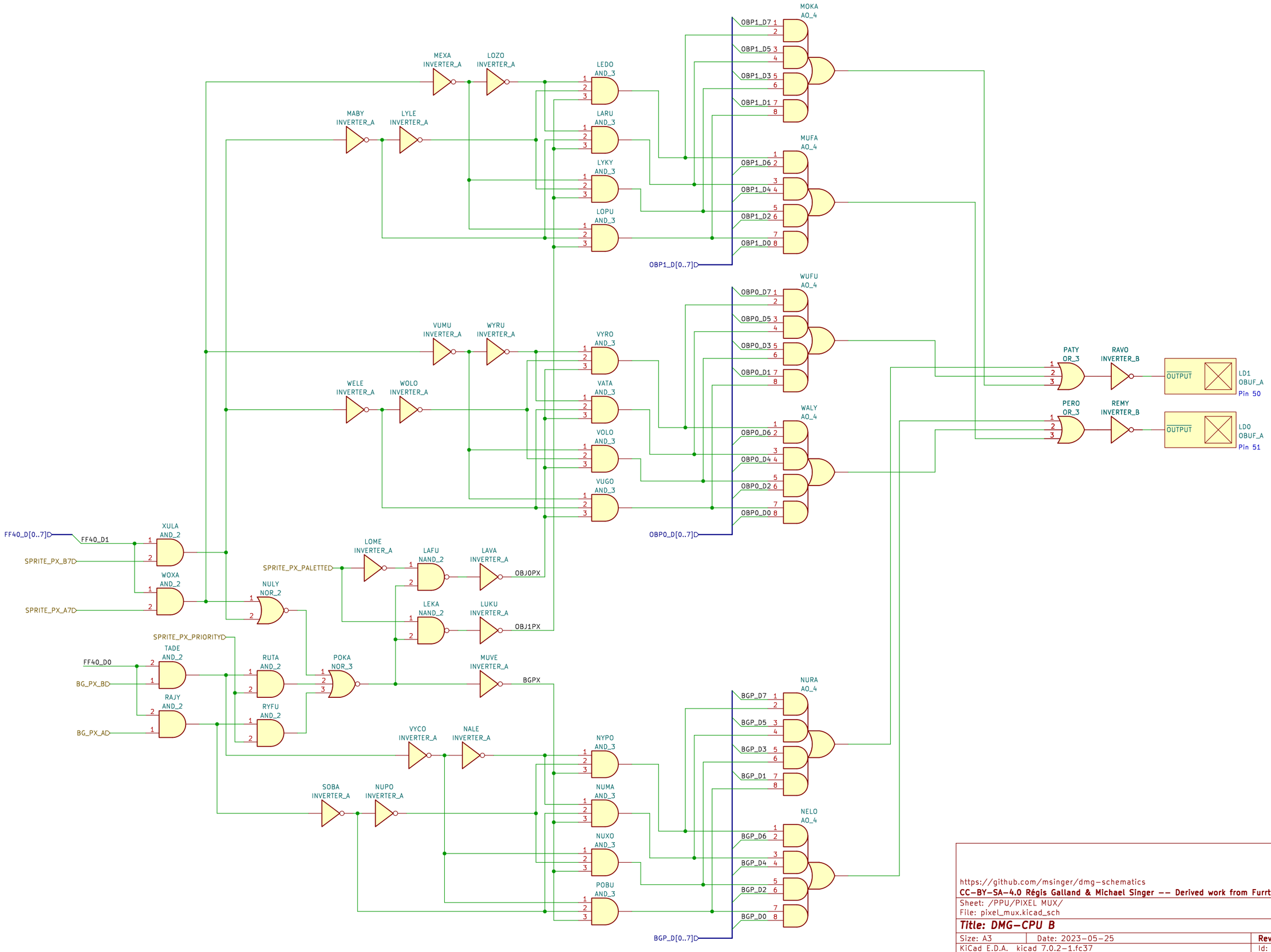
FF48 OBP0



FF49 OBP1



Sheet: /PPU/FF47-FF49 PALETTES/		
File: palettes.kicad_sch		
Title: DMG-CPU B		
Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 45/46



https://github.com/msinger/dmg-schematics

Sheet: /PPU/PIXEL MUX/
File: pixel_mux.kicad_sch

Title: DMG-CPU B

Size: A3	Date: 2023-05-25	**Rev: 0.6**
KiCad E.D.A. kicad 7.0.2-1.fc37		Id: 46/46